DLP® Digital Controller for the DLP3000 DMD

Check for Samples: DLPC300

FEATURES

- **Supports Reliable Operation of the DLP3000 DMD**
- **Multi-Mode, 24-Bit Input Port:**
  - **Supports Parallel RGB With Pixel Clock Up to 33.5 MHz and 3 Input Color Bit-Depth Options:**
    - **24-Bit RGB888 or 4:4:4 YCrCb888**
    - **18-Bit RGB666 or 4:4:4 YCrCb666**
    - **16-Bit RGB565 or 4:2:2 YCrCb565**
  - **Supports 8-Bit BT.656 Bus Mode With Pixel Clock Up to 33.5 MHz**
- **Supports Input Resolutions 608x684, 854x480 (WVGA), 640x480 (VGA), 320x240 (QVGA)**
- **Pattern Input Mode**
  - **One-to-One Mapping of Input Data to Micromirrors**
  - **1-Bit Binary Pattern Rates up to 4000-Hz**
  - **8-Bit Grayscale Pattern Rates up to 120-Hz**
- **Video Input Mode with Pixel Data Processing**
  - **Supports 1Hz to 60Hz Frame Rates**
  - **Programmable Degamma**
  - **Spatial-Temporal Multiplexing (Dithering)**
  - **Automatic Gain Control**
  - **Color Space Conversion**
- **Output Trigger Signal for Synchronizing with Camera, Sensor, or Other Peripherals**
- **System Control:**
  - **I^2C Control of Device Configuration**
  - **Programmable Current Control of up to 3 LEDs**
  - **Integrated DMD Reset Driver Control**
  - **DMD Horizontal and Vertical Display Image Flip**
- **Low Power Consumption: Only 93 mW (Typical)**
- **External Memory Support:**
  - **166-MHz Mobile DDR SDRAM**
  - **33.3-MHz Serial FLASH**
- **176-Pin, 7 × 7 mm with 0.4-mm Pitch VFBGA Package**

APPLICATIONS

- **Machine Vision**
- **Industrial Inline Inspection**
- **3D Scanning**
- **3D Optical Metrology**
- **Automated Fingerprint Identification**
- **Face Recognition**
- **Augmented Reality**
- **Embedded Display**
- **Interactive Display**
- **Information Overlay**
- **Spectroscopy**
- **Chemical Analyzers**
- **Medical Instruments**
- **Photo-Stimulation**
- **Virtual Gauges**

DESCRIPTION

The DLPC300 digital controller, part of the DLP 0.3 WVGA chipset, supports reliable operation of the DLP3000 DMD. The DLPC300 controller also provides a convenient, multi-functional interface between user electronics and the DMD, enabling high-speed pattern rates (up to 4 kHz binary), providing LED control and data formatting for multiple input resolutions. The DLPC300 also outputs a trigger signal for synchronizing displayed patterns with a camera, sensor, or other peripherals.

The DLPC300 controller enables integration of the DLP 0.3 WVGA chipset into small-form-factor and low-cost light steering applications. Example end equipments for the 0.3 WVGA chipset include 3D scanning or metrology systems with structured light, interactive displays, chemical analyzers, medical instruments, and other end equipments requiring spatial light modulation (or light steering and patterning).

The DLPC300 is one of the two devices in the 0.3 WVGA chipset (see Figure 1). The other device is the DLP3000 DMD. After RESET is released, the DLPC300 controller reads the configuration information stored in the serial FLASH. The configuration information is available for download from DLPR300 product folder. See the *0.3 WVGA Chip-Set* data sheet (TI literature number DLPZ005) for further details.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

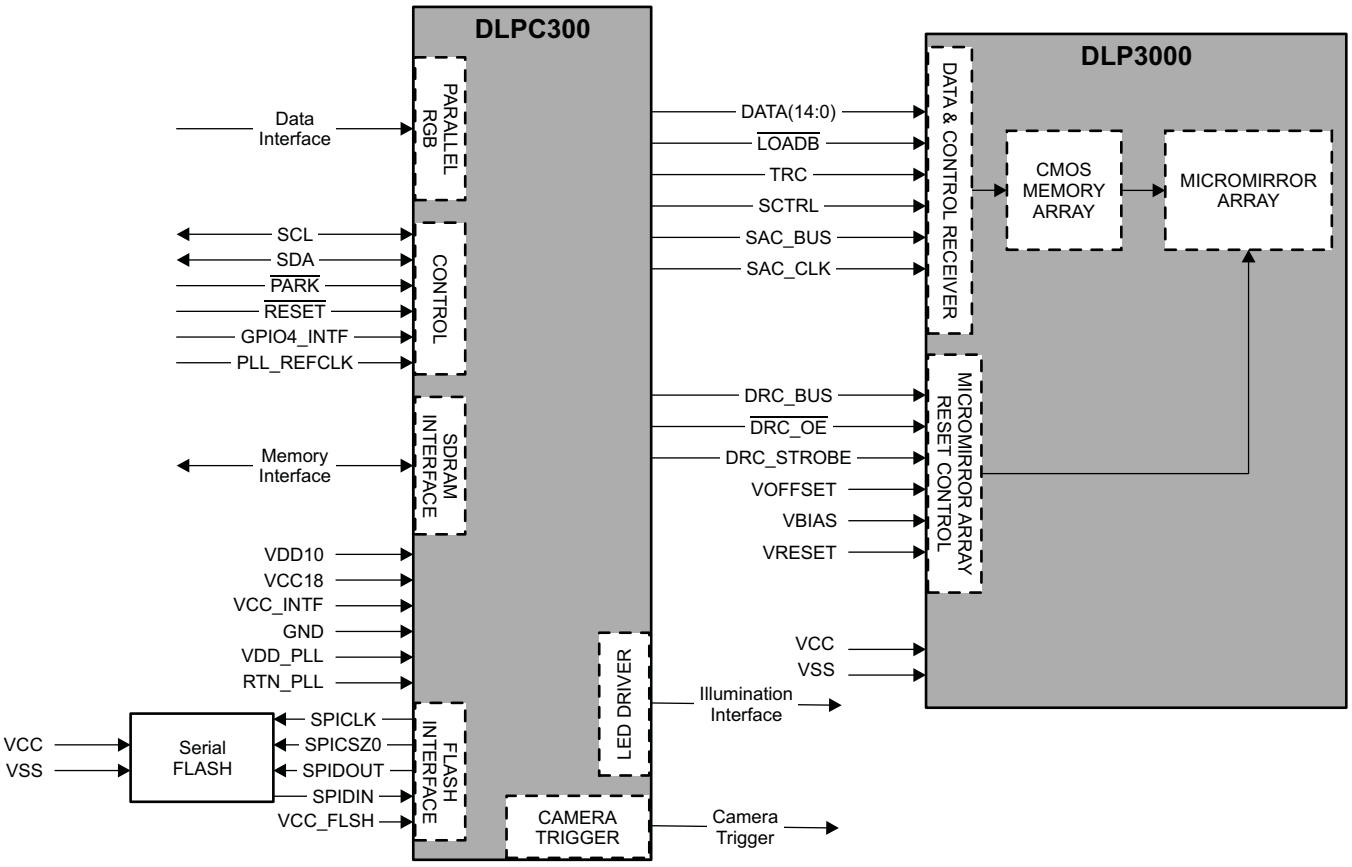


Figure 1. Chipset Block Diagram

In DLP-based solutions, image data is 100% digital from the DLPC300 input port to the image on the DMD. The image stays in digital form and is never converted into an analog signal. The DLPC300 processes the digital input image and converts the data into a format needed by the DLP3000. The DLP3000 then steers light by using binary pulse-width-modulation (PWM) for each pixel mirror. Refer to DLP3000 Data Sheet (TI literature number DLPS022) for further details.

Figure 2 is the DLPC300 functional block diagram. As part of the pixel processing functions, the DLPC300 offers format conversion functions: chroma interpolation for 4:2:2 and 4:4:4, color-space conversion, and gamma correction. The DLPC300 also offers several image-enhancement functions: programmable degamma, automatic gain control, and image resizing. Additionally, the DLPC300 offers an artifact migration function through spatial-temporal multiplexing (dithering). Finally, the DLPC300 offers the necessary functions to format the input data to the DMD. The pixel processing functions allow the DLPC300 and DLP3000 to support a wide variety of resolutions including NTSC, PAL, QVGA, QWVGA, VGA, and WVGA. The pixel processing functions can be optionally bypassed with the native 608 × 684 pixel resolution.

When accurate pattern display is needed, the native 608x684 input resolution pattern has a one-to-one association with the corresponding micromirror on the DLP3000. The DLPC300 enables high-speed display of these patterns: up to 1440 Hz for binary (1-Bit) patterns and up to 120 Hz for 8-Bit patterns. This functionality is well-suited for techniques such as structured light, rapid manufacturing, or digital exposure.

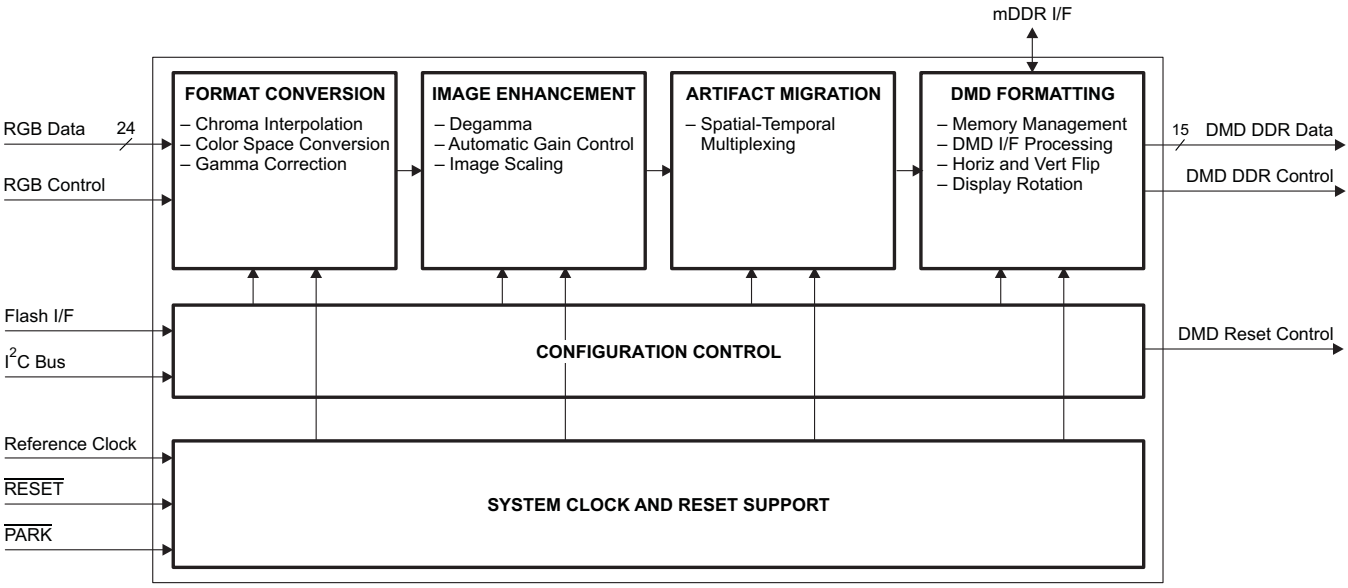


Figure 2. DLPC300 Functional Block Diagram

Commands can be input to the DLPC300 over an I^2C interface.

The DLPC300 takes as input 16-, 18- or 24-bit RGB data at up to 60-Hz frame rate. This frame rate is composed of three colors (red, green, and blue) with each color equally divided in the 60-Hz frame rate. Thus, each color has a 5.55 ms time slot allocated. Because each color has 5-, 6-, or 8-bit depth, each color time slot is further divided into bit-planes. A bit-plane consists of a one-bit representation of all the pixels in the image. See Figure 3.

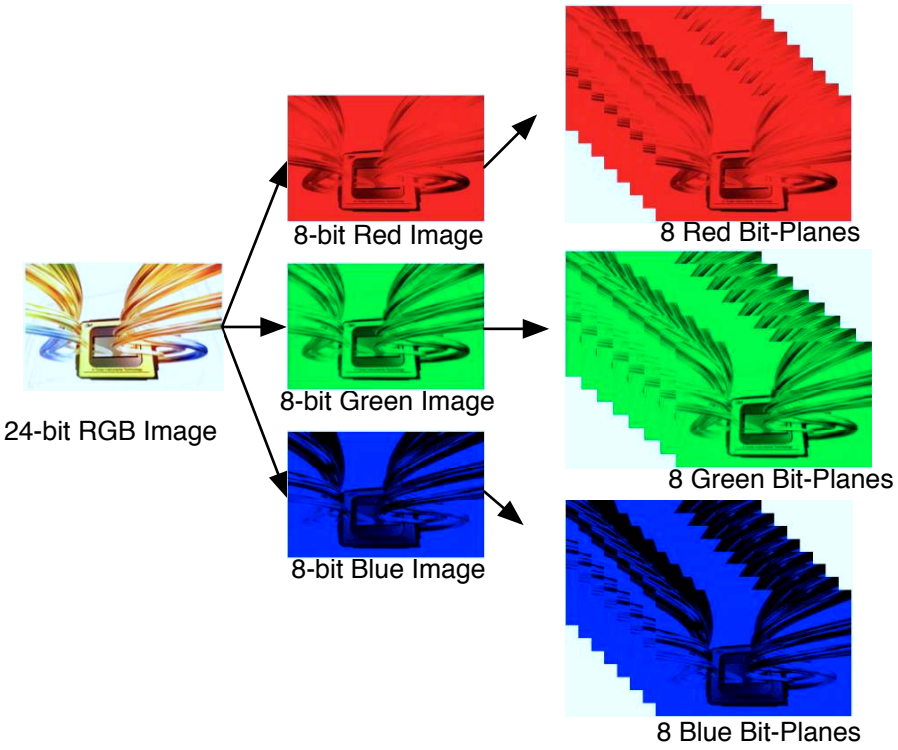


Figure 3. Bit Slices

The length of each bit-plane in the time slot is weighted by the corresponding power of 2 of its binary representation. This provides a binary pulse-width modulation of the image. For example, a 24-bit RGB input has three colors with 8-bit depth each. Each color time slot is divided into eight bit-planes, with the sum of all bit planes in the time slot equal to 256. See Figure 4 for an illustration of this partition of the bits in a frame.

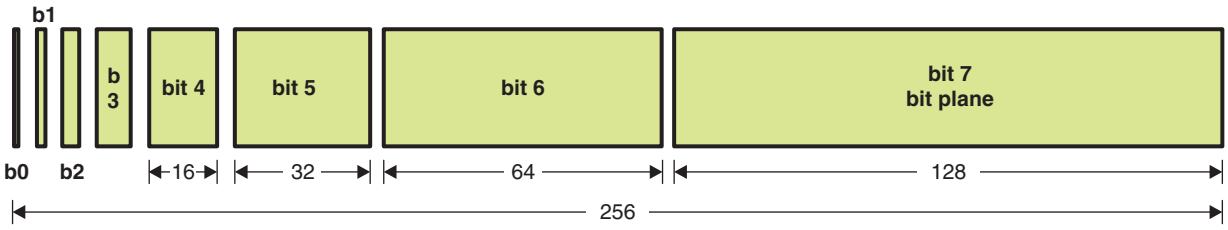


Figure 4. Bit Partition in a Frame for an 8-Bit Color

Therefore, a single video frame is composed of a series of bit-planes. Because the DMD mirrors can be either on or off, an image is created by turning on the mirrors corresponding to the bit set in a bit-plane. With the binary pulse-width modulation, the intensity level of the color is reproduced by controlling the amount of time the mirror is on. For a 24-bit RGB frame image inputted to the DLP300, the DLPC300 creates twenty-four bit planes, stores them on the mDDR, and sends them to the DLP3000 DMD, one bit-plane at a time. Depending on the bit weight of the bit-plane, the DLPC300 controls the time this bit-plane is exposed to light, controlling the intensity of the bit-plane. To improve image quality in video frames, these bit-planes, time slots, and color frames are intertwined and interleaved with spatial-temporal algorithms by the DLPC300.

For other applications where this image enhancement is not desired, the video processing algorithms can be bypassed and replaced with a specific set of bit-planes. The bit-depth of the pattern is then allocated into the corresponding time slots. Futhermore, an output trigger signal is also synchronized with these time slots to indicate when the image is displayed. For structured light applications this mechanism provides the capability to display a set of patterns and signal a camera to capture these patterns overlayed on an object.

Figure 5 illustrates the bit planes and corresponding output triggers for 3-bit, 6-bit, and 12-bit RBG. Table 1 shows the allowed pattern combinations in relation to the bit depth of the pattern.

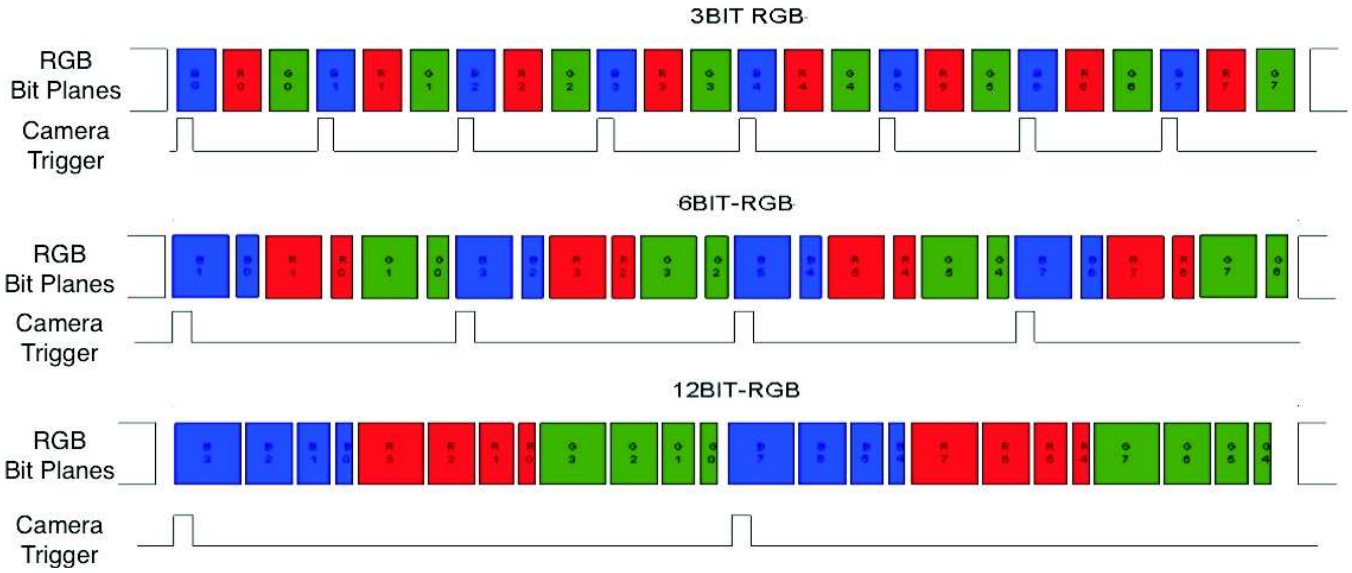


Figure 5. Bit Planes and Output Trigger for 3-, 6-, and 12-Bit RGB Input

Table 1. Allowed Pattern Combinations

COLOR MODE		NUMBER OF PATTERNS PER FRAME	FRAME RATE	PATTERN RATE
Monochrome	1 bit per pixel	24	15, 30, 45, or 60 Hz	24 × Frame Rate
	2 bits per pixel	12		12 × Frame Rate
	3 bits per pixel	8		8 × Frame Rate
	4 bits per pixel	6		6 × Frame Rate
	5 bits per pixel	4		4 × Frame Rate
	6 bits per pixel	4		4 × Frame Rate
	7 bits per pixel	3		3 × Frame Rate
	8 bits per pixel	2		2 × Frame Rate
RGB	1-bit per color pixel (3-bit per pixel)	24		4 × Frame Rate
	2-bit per color pixel (6-bit per pixel)	12		3 × Frame Rate
	4-bit per color pixel (12-bit per pixel)	8		2 × Frame Rate
	8-bit per color pixel (24-bit per pixel)	1		Frame Rate

An optional FPGA (see the DLPR300 Software Folder) can be added to the system to manage the bit-planes stored in the mDDR. The mDDR accomodates four 608 × 684 images of 24-bit RGB data or 96 bit-planes (24 bit-planes × 4 images). By pre-loading the mDDR with these bit-planes, faster frame rates can be achieved. The 96 bit-plane buffer is arranged in a circular buffer style, meaning that the last bit-plane addition to the buffer replaces the oldest stored bit-plane. Figure 6 shows the overall system with the optional FPGA.

With this FPGA, the pattern frame rate can be calculated with the following equation:

$$\text{pattern rate} = \frac{1}{\text{(pattern exposure period)}} + \text{(bit plane load time)} + \text{(buffer rotate overhead)} \quad (1)$$

where:

typical bit plane load time = 230 µs

typical buffer rotate overhead = 135 µs

Table 2 shows the maximum pattern rate that can be achieved by using a single FPGA internal buffer in continuous mode.

Table 2. Maximum Pattern Rate with Optional FPGA

COLOR MODE		MAXIMUM NUMBER OF PATTERNS	MAXIMUM PATTERN RATE
Monochrome	1 bit per pixel	96	4000 Hz
	2 bits per pixel	48	1600 Hz
	3 bits per pixel	32	480 Hz
	4 bits per pixel	24	360 Hz
	5 bits per pixel	16	240 Hz
	6 bits per pixel	16	240 Hz
	7 bits per pixel	12	180 Hz
	8 bits per pixel	12	120 Hz

Figure 6 illustrates the chipset with the optional FPGA.

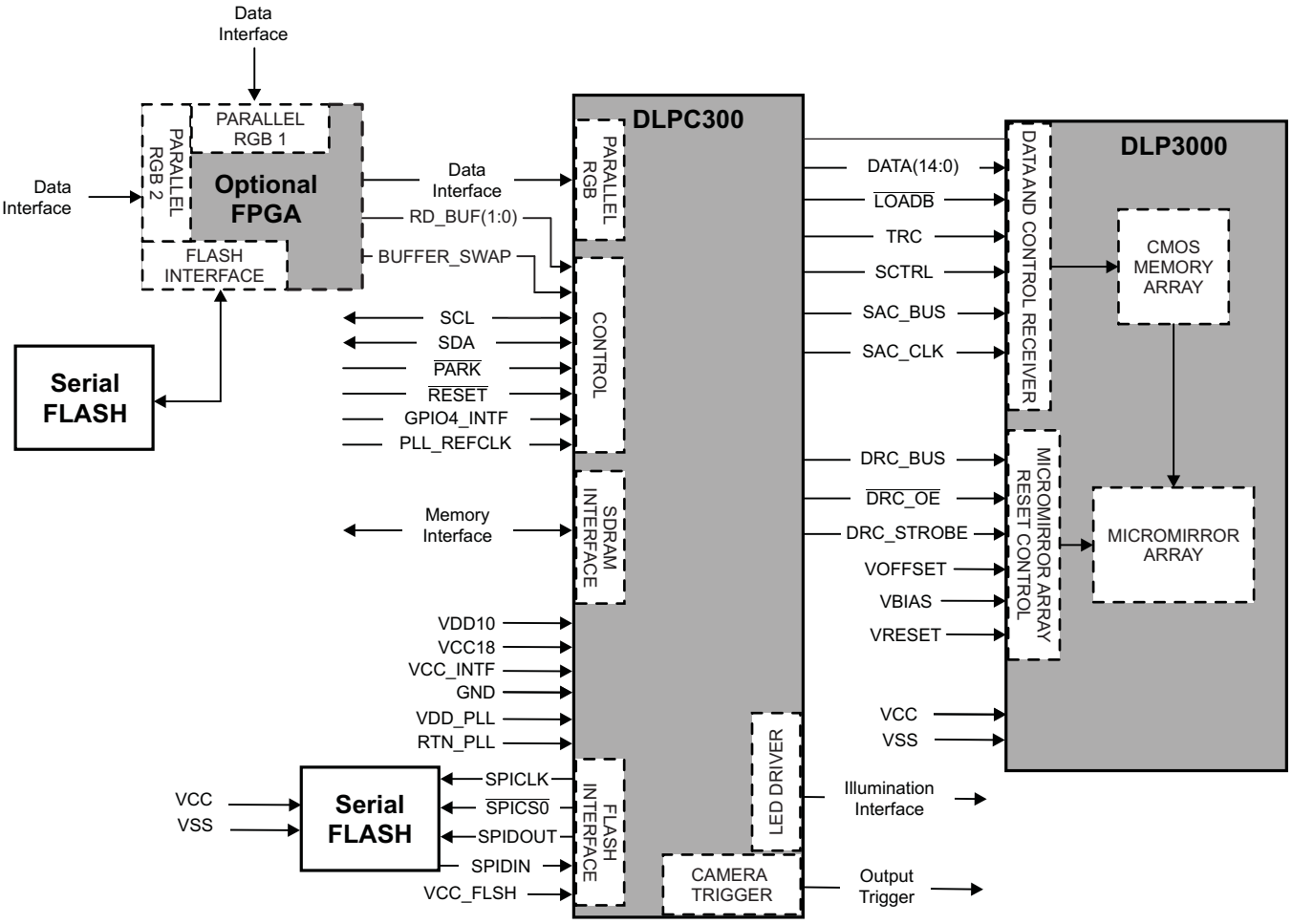


Figure 6. DLP3000 Chipset With Optional FPGA

The digital RGB input interface operates at 1.8 V, 2.5 V, or 3.3 V nominal, depending on the VCC_INTF supply. The SPI flash interface operates at 1.8 V, 2.5 V, or 3.3 V nominal, depending on the VCC_FLSH supply. The DMD and mDDR interface operates at 1.8 V nominal (VCC18). The core transistors operates at 1 V nominal (VDD10). The analog PLL operates at 1 V nominal (VDD_PLL).

Typical System Application

A typical embedded system application using the DLPC300 is shown in Figure 7. In this configuration, the DLPC300 controller supports a 24-bit parallel RGB, typical of LCD interfaces, from the main processor chip. This system supports both still and motion video sources. For this configuration, the controller only supports periodic sources. This is ideal for motion video sources, but can also be used for *still images* by maintaining periodic syncs but only sending a frame of data when needed. The *still image* must be fully contained within a single video frame and meet frame timing constraints. The DLPC300 refreshes the displayed image at the source frame rate and repeats the last active frame for intervals in which no new frame has been received.

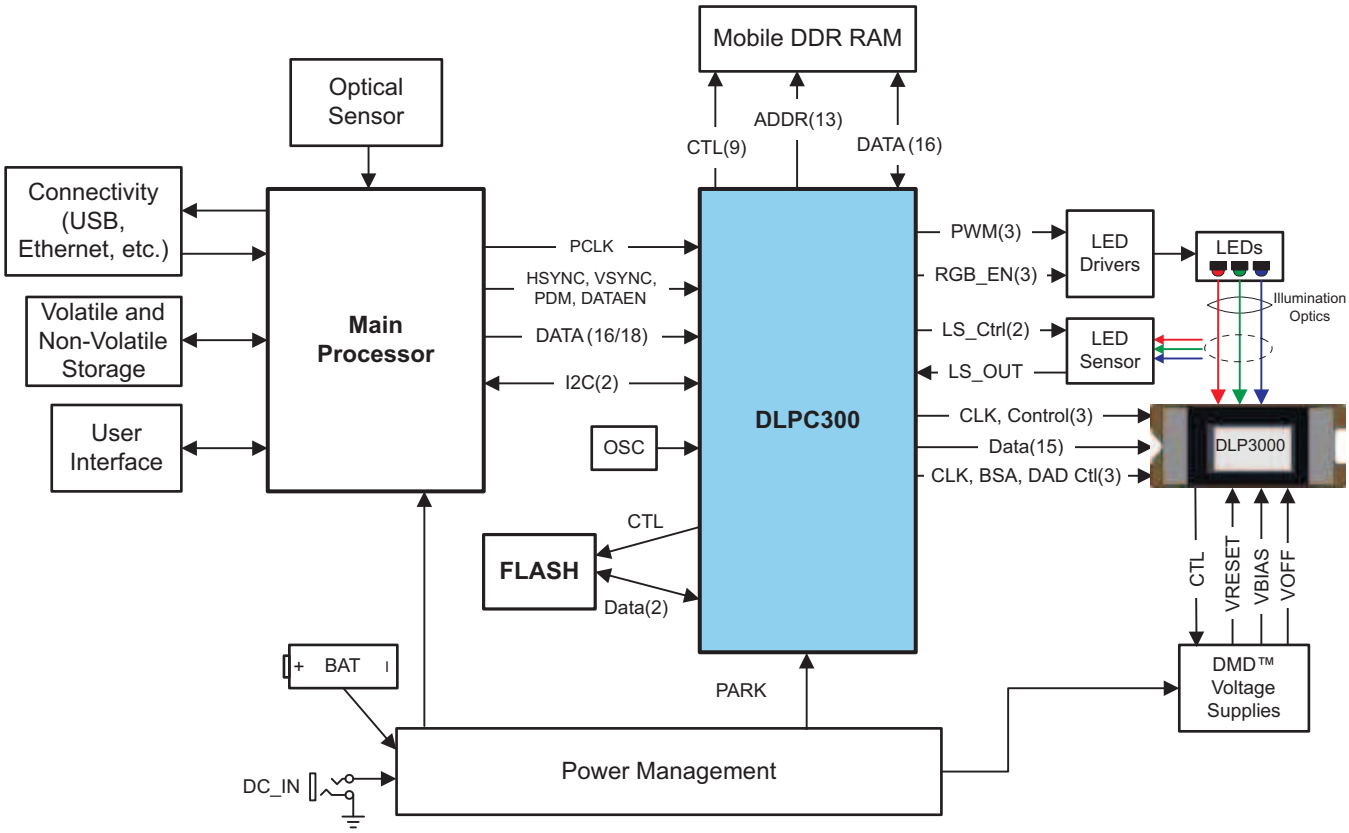


Figure 7. Typical Embedded System Block Diagram

Related Documents

DOCUMENT	TI LITERATURE NUMBER
DLP3000 0.3 WVGA Series 220 DMD data sheet	DLPS022
DLP® 0.3 WVGA Chipset	DLPZ005
DLPC300 Programmer's Guide	DLPU004

Device Part Number Nomenclature

Figure 8 provides a legend for reading the complete device name for any DLP device.

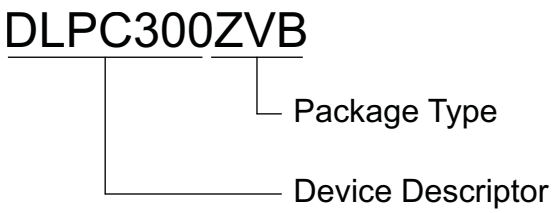


Figure 8. Device Nomenclature

Device Marking

The device marking consists of the fields shown in Figure 9.

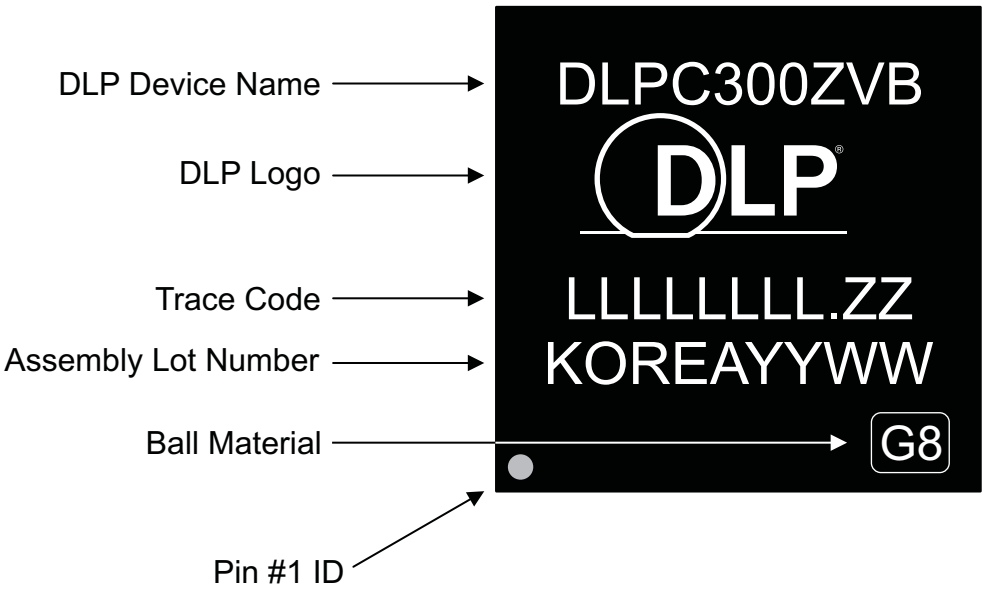


Figure 9. Device Marking

SIGNAL FUNCTIONAL DESCRIPTIONS

This section describes the input/output characteristics of signals that interface to the DLPC300 by functional groups. Table 3 includes I/O power and type characteristic references which are further described in subsequent sections.

Table 3. Functional Pin Descriptions

TERMINAL		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NO.				
$\overline{\text{RESET}}$	J14	VCC18	I_1	Async	DLPC300 power-on reset. Self configuration starts when a low-to-high transition is detected on this pin. All device power and clocks must be stable and within recommended operating conditions before this reset is de-asserted. Note that the following 7 signals are high-impedance while $\overline{\text{RESET}}$ is asserted: DMD_PWR_EN, LEDDVR_ON, LED_SEL_0, LED_SEL_1, SPICLK, SPIDOUT, $\overline{\text{SPICS0}}$ External pullups/-downs should be added as needed to these signals to avoid floating inputs where these signals are driven.
$\overline{\text{PARK}}$	B8	VCC_ INTF	I_3	Async	DMD park control (active-low). Is set high to enable normal operation. $\overline{\text{PARK}}$ must be set high within 500 µs after releasing $\overline{\text{RESET}}$. $\overline{\text{PARK}}$ must be set low a minimum of 500 µs before any power is to be removed from the DLPC300 or DLP3000. See *System Power-Up/Down Sequence* for more details.
PLL_REFCLK_I	K15	VCC18 (filter)	I_4	N/A	Reference clock crystal Input. If an external oscillator is used in place of a crystal, then this pin should be used as the oscillator input.
PLL_REFCLK_O	J15	VCC18 (filter)	O_{14}	N/A	Reference clock crystal return. If an external oscillator is used in place of a crystal, then this pin should be left unconnected (floating).
FLASH INTERFACE(1)					
SPICLK	A4	VCC_FLSH	O_{24}	N/A	SPI Master Clock output.

(1) Each device connected to the SPI bus must operate from VCC_FLSH.

Table 3. Functional Pin Descriptions (continued)

TERMINAL NAME	TERMINAL NO.	I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION	
SPIDIN	B4	VCC_FLSH	I_2	SPICLK	Serial data input from the external SPI slave FLASH device.	
$\overline{\text{SPICS0}}$	A5	VCC_FLSH	O_{24}	SPICLK	SPI Master Chip Select 0 output. Active-low	
RESERVED	C6	VCC_FLSH	O_{24}	SPICLK	Not used. Reserved for future use. Should be left unconnected	
SPIDOUT	C5	VCC_FLSH	O_{24}	SPICLK	Serial data output to the external SPI slave FLASH device. This pin sends address and control information as well as data when programming.	
CONTROL						
RESERVED0	B10	VCC_ INTF	I_3	SCL	Not used. Reserved for future use. Should be pulled up to VCC_INTF.	
SCL	A10	VCC_ INTF	B_{38}	N/A	I^2C clock. Bidirectional, open-drain signal. An external pull-up is required. No I^2C activity is permitted for a minimum of 100 ms after $\overline{\text{PARK}}$ and $\overline{\text{RESET}}$ are set high.	
SDA	C10	VCC_ INTF	B_{38}	SCL	I^2C data. Bidirectional, open-drain signal. An external pull-up is required.	
GPIO4_INTF	C9	VCC_ INTF	B_{34}	Async	General-purpose I/O 4. Primary usage is to indicate when auto-initialization is complete (also called INIT-DONE, which is when GPIO4 transitions high then low following release of $\overline{\text{RESET}}$) and to flag a detected error condition in the form of a logic-high, pulsed interrupt flag subsequent to INIT-DONE.	
RESERVED1	B9	VCC_ INTF	B_{34}	Async	Reserved for future use. This pin should be left unconnected.	
PARALLEL RGB INTERFACE					**PARALLEL RGB MODE**	**BT.656 I/F MODE**
PCLK	D13	VCC_ INTF	I_3	N/A	Pixel clock(2)	Pixel clock(2)
PDM	H15	VCC_ INTF	B34	ASYNC	Not used, pull-down through an external resistor.	Not used, pull-down through an external resistor.
VSYNC	H14	VCC_ INTF	I_3	ASYNC	VSync(3)	Unused(4)
HSYNC	H13	VCC_ INTF	I_3	PCLK	HSync (3)	Unused(4)
DATEN	G15	VCC_ INTF	I_3	PCLK	Data valid(2)	Unused(4)
PDATA[0]	G14	VCC_ INTF	I_3	PCLK	Data0(5)	Data0(5)
PDATA[1]	G13	VCC_ INTF	I_3	PCLK	Data1 (5)	Data1 (5)
PDATA[2]	F15	VCC_ INTF	I_3	PCLK	Data2 (5)	Data2 (5)
PDATA[3]	F14	VCC_ INTF	I_3	PCLK	Data3 (5)	Data3 (5)
PDATA[4]	F13	VCC_ INTF	I_3	PCLK	Data4(5)	Data4(5)
PDATA[5]	E15	VCC_ INTF	I_3	PCLK	Data5 (5)	Data5 (5)
PDATA[6]	E14	VCC_ INTF	I_3	PCLK	Data6 (5)	Data6 (5)
PDATA[7]	E13	VCC_ INTF	I_3	PCLK	Data7(5)	Data7(5)
PDATA[8]	D15	VCC_ INTF	I_3	PCLK	Data8(5)	Unused(4)
PDATA[9]	D14	VCC_ INTF	I_3	PCLK	Data9 (5)	Unused(4)
PDATA[10]	C15	VCC_ INTF	I_3	PCLK	Data10 (5)	Unused(4)
PDATA[11]	C14	VCC_ INTF	I_3	PCLK	Data11(5)	Unused(4)
PDATA[12]	C13	VCC_ INTF	I_3	PCLK	Data12 (5)	Unused(4)
PDATA[13]	B15	VCC_ INTF	I_3	PCLK	Data13 (5)	Unused(4)
PDATA[14]	B14	VCC_ INTF	I_3	PCLK	Data14 (5)	Unused(4)
PDATA[15]	A15	VCC_ INTF	I_3	PCLK	Data15(5)	Unused(4)

(2) Pixel clock capture edge is SW programmable.
(3) VSYNC, HSYNC and data valid polarity is SW programmable.
(4) Unused inputs should be pulled down to ground through an external resistor.
(5) PDATA[23:0] bus mapping is pixel-format and source-mode dependent. See later sections for details.

Table 3. Functional Pin Descriptions (continued)

TERMINAL		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION	
NAME	NO.					
PDATA[16]	A14	VCC_ INTF	I_3	PCLK	Data16[5]	Unused[4]
PDATA[17]	B13	VCC_ INTF	I_3	PCLK	Data17[5]	Unused[4]
PDATA[18]	A13	VCC_ INTF	I_3	PCLK	Data18[5]	Unused[4]
PDATA[19]	C12	VCC_ INTF	I_3	PCLK	Data19[5]	Unused[4]
PDATA[20]	B12	VCC_ INTF	I_3	PCLK	Data20[5]	Unused[4]
PDATA[21]	A12	VCC_ INTF	I_3	PCLK	Data21[5]	Unused[4]
PDATA[22]	C11	VCC_ INTF	I_3	PCLK	Data22[5]	Unused[4]
PDATA[23]	B11	VCC_ INTF	I_3	PCLK	Data23[5]	Unused[4]

Table 3. Functional Pin Descriptions (continued)

TERMINAL		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NO.				
DMD INTERFACE					
DMD_D0	M15	VCC18	O_{58}	DMD_DCLK	DMD data pins. DMD data pins are double data rate (DDR) signals that are clocked on both edges of DMD_DCLK. All 15 DMD data signals are use to interface to the DLP3000.
DMD_D1	N14				
DMD_D2	M14				
DMD_D3	N15				
DMD_D4	P13				
DMD_D5	P14				
DMD_D6	P15				
DMD_D7	R15				
DMD_D8	R12 d				
DMD_D9	N11				
DMD_D10	P11				
DMD_D11	R11				
DMD_D12	N10				
DMD_D13	P10				
DMD_D14	R10				
DMD_DCLK	N13	VCC18	O_{58}	N/A	DMD data clock (DDR)
$\overline{\text{DMD\_LOADB}}$	R13	VCC18	O_{58}	DMD_DCLK	DMD data load signal (active-low). This signal requires an external pullup to VCC18.
DMD_SCTRL	R14	VCC18	O_{58}	DMD_DCLK	DMD data serial control signal
DMD_TRC	P12	VCC18	O_{58}	DMD_DCLK	DMD data toggle rate control
DMD_DRC_BUS	L13	VCC18	O_{58}	DMD_SAC_CLK	DMD reset control bus data
DMD_DRC_STRB	K13	VCC18	O_{58}	DMD_SAC_CLK	DMD reset control bus strobe
$\overline{\text{DMD\_DRC\_OE}}$	M13	VCC18	O_{58}	Async	DMD reset control enable (active-low). This signal requires an external pullup to VCC18.
DMD_SAC_BUS	L15	VCC18	O_{58}	DMD_SAC_CLK	DMD stepped-address control bus data
DMD_SAC_CLK	L14	VCC18	O_{58}	N/A	DMD stepped-address control bus clock
DMD_PWR_EN	K14	VCC18	O_{14}	Async	DMD power regulator enable (active-high). This is an active-high output that should be used to control DMD V_{OFFSET}, V_{BIAS}, and V_{RESET} voltages. DMD_PWR_EN is driven high as a result of the $\overline{\text{PARK}}$ input signal being set high. However, DMD_PWR_EN is held high for 500 µs after the $\overline{\text{PARK}}$ input signal is set low before it is driven low. A weak external pulldown resistor is recommended to keep this signal at a known state during power-up reset.

Table 3. Functional Pin Descriptions (continued)

TERMINAL		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NO.				
SDRAM INTERFACE					
MEM_CLK_P	D1	VCC18	O_{74}	N/A	mDDR memory, differential memory clock
MEM_CLK_N	E1	VCC18	O_{74}	N/A	
MEM_A0	P1	VCC18	O_{64}	MEM_CLK	mDDR memory, multiplexed row and column address
MEM_A1	R3				
MEM_A2	R1				
MEM_A3	R2				
MEM_A4	A1				
MEM_A5	B1				
MEM_A6	A2				
MEM_A7	B2				
MEM_A8	D2				
MEM_A9	A3				
MEM_A10	P2				
MEM_A11	B3				
MEM_A12	D3				
MEM_BA0	M3	VCC18	O_{64}	MEM_CLK	mDDR memory, bank select
MEM_BA1	P3				
$\overline{\text{MEM\_RAS}}$	P4	VCC18	O_{64}	MEM_CLK	mDDR memory, row address strobe (active-low)
$\overline{\text{MEM\_CAS}}$	R4	VCC18	O_{64}	MEM_CLK	mDDR memory, column address strobe (active-low)
$\overline{\text{MEM\_WE}}$	R5	VCC18	O_{64}	MEM_CLK	mDDR memory, write enable (active-low)
$\overline{\text{MEM\_CS}}$	J3	VCC18	O_{64}	MEM_CLK	mDDR memory, chip select (active-low)
MEM_CKE	C1	VCC18	O_{64}	MEM_CLK	mDDR memory, clock enable (active-high)
MEM_LDQS	J2	VCC18	B_{64}	N/A	mDDR memory, lower byte, R/W data strobe
MEM_LDM	J1	VCC18	O_{64}	MEM_LDQS	mDDR memory, lower byte, write data mask
MEM_UDQS	G1	VCC18	B_{64}	N/A	mDDR memory, upper byte, R/W data strobe
MEM_UDM	H1	VCC18	O_{64}	MEM_UDQS	mDDR memory, upper byte, write data mask
MEM_DQ0	N1	VCC18	B_{64}	MEM_LDQS	mDDR memory, lower byte, bidirectional R/W data
MEM_DQ1	M2				
MEM_DQ2	M1				
MEM_DQ3	L3				
MEM_DQ4	L2				
MEM_DQ5	K2				
MEM_DQ6	L1				
MEM_DQ7	K1				
MEM_DQ8	H2	VCC18	B_{64}	MEM_UDQS	mDDR memory, upper byte, bidirectional R/W data
MEM_DQ9	G2				
MEM_DQ10	H3				
MEM_DQ11	F3				
MEM_DQ12	F1				
MEM_DQ13	E2				
MEM_DQ14	F2				
MEM_DQ15	E3				

Table 3. Functional Pin Descriptions (continued)

TERMINAL NAME	TERMINAL NO.	I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
LED DRIVER INTERFACE					
RPWM	N8	VCC18	O_{14}	Async	Red LED PWM signal used to control the LED current(6).
GPWM	P9	VCC18	O_{14}	Async	Green LED PWM signal used to control the LED current(6).
BPWM	R8	VCC18	O_{14}	Async	Blue LED PWM signal used to control the LED current(6).
LED_SEL_0	R6	VCC18	O_{14}	Async	LED enable SELECT. Controlled by DMD sequence timing. LED_SEL(1:0) Selected LED 00 None 01 Red 10 Green 11 Blue A decode circuit is required to decode the selected LED enable.
LED_SEL_1	N6				
LEDDRV_ON	P7	VCC18	O_{14}	Async	LED driver master enable. Active-high output control to external LED driver logic. This signal is driven high 100 ms after LED_ENABLE is driven high. Driven low immediately when either LED_ENABLE or PARK is driven low.
LED_ENABLE	A11	VCC_ INTF	I_3	Async	LED enable (active-high input). A logic low on this signal forces LEDDRV_ON low and LED_SEL(1:0) = 00b. These signals are enabled 100 ms after LED_ENABLE transitions from low to high.
RED_EN	B5	VCC18	B_{18}	Async	When not used with an optional FPGA, this signal should be connected to the RED LED enable circuit. When RED_EN is high, the red LED is enabled. When RED_EN is low, the red LED is disabled. When used with the optional FPGA, this signal should be pulled down to ground through an external resistor. This signal is configured as output when the DLPR300 serial FLASH PROM is loaded by the DLPC300.
GREEN_EN	A7				When not used with an optional FPGA, this signal should be connected to the green LED enable circuit. When GREEN_EN is high, the green LED is enabled. When GREEN_EN is low, the green LED is disabled. When used with the optional FPGA, this signal should be pulled down to ground through an external resistor. This signal is configured as output when the DLPR300 serial FLASH PROM is loaded by the DLPC300.
BLUE_EN	C8				When not used with an optional FPGA, this signal should be connected to the blue LED enable circuit. When BLUE_EN is high, the blue LED is enabled. When BLUE_EN is low, the blue LED is disabled. When used with the optional FPGA, this signal should be pulled down to ground through an external resistor. This signal is configured as output when the DLPR300 serial FLASH PROM is loaded by the DLPC300.
WHITE POINT CORRECTION LIGHT SENSOR I/F					
CMP_OUT	A6	VCC18	I_1	Async	Successive approximation ADC comparator output (DLPC300 input). Assumes a successive approximation ADC is implemented with a light sensor and/or thermocouple feeding one input of an external comparator and the other side of the comparator driven from the DLPC300 CMP_PWM pin. If not used, this signal should be pulled down to ground .

(6) All LED PWM signals are forced high when LEDDRV_ON = 0, SW LED control is disabled, or the sequence stops.

Table 3. Functional Pin Descriptions (continued)

TERMINAL NAME	TERMINAL NO.	I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
CMP_PWM	B7	VCC18	O_{14}	Async	Successive approximation comparator pulse-width modulation input. Supplies a PWM signal to drive the successive approximation ADC comparator used in light-to-voltage light sensor applications. Should be left unconnected if this function is not used.
GPIO0_CMPPWR	P5	VCC18	B_{14}	Async	Power control signal for the WPC light sensor and other analog support circuits using the DLPC300 ADC. Alternatively, it provides general purpose I/O to the WPC microprocessor internal to the DLPC300. Should be left unconnected if not used.
TRIGGER CONTROL					
OUTPUT_TRIGGER	N9	VCC18	B_{18}	Async	Trigger output. Indicates that a pattern or image is displayed on the screen and is ready to be captured. With an optional FPGA, this signal is connected to the FPGA trigger input. This signal is configured as output when the DLPR300 serial FLASH PROM is loaded by the DLPC300. If not used, this signal should be should be pulled down to ground through an external resistor.
PATTERN CONTROL					
PATTERN_INVERT	C7	VCC18	B_{18}	Async	Inverts the current 1-bit pattern held in the DLPC300 buffer. When used with an optional FPGA, this signal should be connected to DMC_TRC of the FPGA. This signal is configured as output when the DLPR300 serial FLASH PROM is loaded by the DLPC300. If not used, this signal should be should be pulled down to ground through an external resistor.
OPTIONAL FPGA BUFFER MANAGEMENT INTERFACES					
RD_BUF0	B6	VCC18	B_{18}	Async	When not used with an optional FPGA, this signal should be should be pulled down to ground through an external resistor. When used with an optional FPGA, this signal should be connected to RD_PTR_SDC[0] of the FPGA. RD_BUFF1 and RD_BUFF0 indicate to the FPGA one of the four buffers currently in use. This signal is configured as output when the DLPR300 serial FLASH PROM is loaded by the DLPC300.
RD_BUF1/I2C_ADDR_SEL	R9				This signal is sampled when $\overline{\text{RESET}}$ is de-asserted to choose between two pre-defined 7-bit I^2C Slave Addresses. If I2C_ADDR_SEL signal is pulled-low, then the DLPC300's I^2Cslave address is 1Bh. If I2C_ADDR_SEL signal is pulled-high, then the DLPC300's I^2C slave address is 1Dh. When used with an optional FPGA, this signal should be connected to RD_PTR_SDC[1] of the FPGA. RD_BUFF1 and RD_BUFF0 indicate to the FPGA one of the four buffers currently in use. This signal is set to input upon de-assertion of $\overline{\text{RESET}}$ and configured as output when the DLPR300 serial FLASH PROM is loaded by the DLPC300.
BUFFER_SWAP	A8				When not used with an optional FPGA, this signal should be should be pulled down to ground through an external resistor. When used with an optional FPGA, this signal should be connected to BUFF_SWAP_SEQ of the FPGA. BUFFER_SWAP indicates to the FPGA when to advance the buffer. This signal is configured as output when the DLPR300 serial FLASH PROM is loaded by the DLPC300.
CONTROLLER MANUFACTURER TEST SUPPORT					
TEST_EN	A9	VCC_INTF	I_3	N/A	Reserved for test. Should be connected directly to ground on the PCB for normal operation. Includes weak internal pulldown

Table 3. Functional Pin Descriptions (continued)

TERMINAL		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NO.				
BOARD LEVEL TEST AND DEBUG					
JTAGTDI	P6	VCC18	I_1	JTAGTCK	JTAG, serial data in. Includes weak internal pullup
JTAGTCK	N5	VCC18	I_1	N/A	JTAG, serial data clock. Includes weak internal pullup
JTAGTMS	N7	VCC18	I_1	JTAGTCK	JTAG, test mode select. Includes weak internal pullup
JTAGTDO	R7	VCC18	I_{14}	JTAGTCK	JTAG, serial data out
$\overline{\text{JTAGRSTZ}}$	P8	VCC18	I_1	ASYNC	JTAG, RESET (active-low). Includes weak internal pullup. This signal must be tied to ground,through an external 15-kΩ or less resistor for normal operation.

Power and Ground Pins

Power and ground connections to the DLPC300 are made up of the groupings shown in Table 4.

Table 4. Power and Ground Pin Descriptions(1)

POWER GROUP	PIN NUMBER(S)	DESCRIPTION
VDD10	D5, D9, F4, F12, J4, J12, M6, M8, M11	1-V core logic power supply (9)
VDD_PLL	H12	1-V power supply for the internal PLL (1)
VCC18	C4, D8, E4, G3, K3, K12, L4, M5, M9, M12, N4, N12	1.8-V power supply for all I/O other than the host/ video interface and the SPI flash buses. (12)
VCC_FLSH	D6	1.8- , 2.5- or 3.3-V power supply for SPI flash bus I/O. (1)
VCC_INTF	D11, E12	1.8- , 2.5- or 3.3-V power supply for all I/Os on the host/video interface (includes I^2C, PDATA, video syncs, $\overline{\text{PARK}}$ and LED_ENABLE pins) (2)
GND	D4, D7, D10, D12, G4, G12, H4, K4, L12, M4, M7, M10	Common ground (12)
RTN_PLL	J13	Analog ground return for the PLL (This should be connected to the common ground GND through a ferrite (1)
Reserved	B10, C2, C3, C6, N2, N3	No connects. Other signals can be routed through these pins (vs going around them) to ease routing if desired (6).

(1) 132 total signal I/O pins, 38 total power/ground pins, 6 total reserved pins

ABSOLUTE MAXIMUM RATING

over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. The Absolute Maximum Ratings are stress ratings only, and functional performance of the device at these or any other conditions beyond those indicated under " Recommended Operating Conditions" is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

PARAMETER		CONDITIONS	MIN	MAX	UNIT
Electrical					
VDD10	Voltage applied to VDD10 (1)		–0.5	1.32	V
VDD_PLL	Voltage applied to VDD_PLL (1)		–0.5	1.32	V
VCC18	Voltage applied to VCC18 (1)		-0.5	2.75	V
VCC_FLSH	Voltage applied to VCC_FLSH (1)		-0.5	3.60	V
VCC_INTF	Voltage applied to VCC_INTF (1)		-0.5	3.60	V
	Voltage applied to all other input terminals (1)		-0.5	3.60	V
Environmental					
T_J	Junction temperature		-30	105	ºC
T_{stg}	Storage temperature		-40	125	ºC
ESD	Electrostatic discharge immunity (2)	Human Body Model (HBM)		2000	V
		Charged Device Model (CDM)		500	V

(1) All voltages referenced to VSS (ground).
(2) Tested in accordance with JESD22-A114-B Electrostatic Discharge (ESD) sensitivity testing Human Body Model (HBM).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT	
Electrical							
VDD10	Core logic supply voltage		0.95	1	1.05	V	
VDD_PLL	Analog PLL supply voltage		0.95	1	1.05	V	
VCC18	I/O supply voltage (except FLASH and 24-bit RGB interface signals)		1.71	1.8	1.89	V	
VCC_FLSH	Configuration and control I/O supply voltage	1.8 V LVCMOS	1.71	1.8	1.89	V	
		2.5 V LVCMOS	2.375	2.5	2.625	V	
		3.3 V LVCMOS	3.135	3.3	3.465	V	
VCC_INTF	24-bit RGB interface supply voltage	1.8 V LVCMOS	1.71	1.8	1.89	V	
		2.5 V LVCMOS	2.375	2.5	2.625	V	
		3.3 V LVCMOS	3.135	3.3	3.465	V	
V_I	Input voltage, all other pins		–0.3		VCCIO (1) + 0.3	V	
V_O	Output voltage, all other pins		0		VCCIO (1)	V	
Environmental							
T_J	Operating junction temperature		–20		85	ºC	

(1) VCCIO represents the actual supply voltage applied to the corresponding I/O.

POWER CONSUMPTION

Table 5 lists the typical current and power consumption of the individual supplies. This table assumes the transfer of a 12 × 6 checkerboard image in 864 × 480 landscape mode at periodic 30 frames per second over the Parallel RGB interface at 25ºC. Note that VCC_FLSH power is zero since the serial FLASH is only accessed upon device configuration and not during normal operation.

Table 5. Power Consumption

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC_INTF	1.8 V		0.1		mW
VCC_FLSH	2.5 V		0		mW
VCC18	1.8 V		50.8		mW
VDD_PLL	1.0 V		2.8		mW
VDD10	1.0 V		39		mW

I/O Characteristics

Voltage and current characteristics for each I/O type signal listed in Table 3, *Functional Pin Descriptions*, are summarized in Table 6. All inputs and outputs are LVCMOS.

Table 6. I/O Characteristics

PARAMETER			CONDITIONS		MIN	MAX	UNIT
V_{IH}	High-level input voltage	B_{64} inputs	V_{CC} = 1.8 V		1.19	V_{CC} + 0.3	V
		I_1, I_2, I_3, I_4, B_{14}, B_{18}, B_{34}, B_{38} inputs			1.2	V_{CC} + 0.3	
		I_2, I_3, B_{34}, B_{38} inputs	V_{CC} = 2.5 V		1.7	V_{CC} + 0.3	
		I_2, I_3, B_{34}, B_{38} inputs	V_{CC} = 3.3 V		2	V_{CC} + 0.3	
V_{IL}	Low-level input voltage	I_1, I_2, I_3, I_4, B_{14}, B_{18}, B_{34}, B_{38} inputs	V_{CC} = 1.8 V		–0.3	0.5	V
		B_{64} inputs			–0.3	0.57	
		I_2, I_3, B_{34}, B_{38} inputs	V_{CC} = 2.5 V		–0.3	0.7	
		I_2, I_3, B_{34}, B_{38} inputs	V_{CC} = 3.3 V		–0.3	0.8	
V_{OH}	High-level output voltage	O_{14}, O_{24}, B_{14}, B_{34} outputs	V_{CC} = 1.8 V,	I_{OH} = –2.58 mA	1.25		V
		O_{58} outputs		I_{OH} = = –6.41 mA	1.25		
		B_{18}, B_{38} outputs		I_{OH} = = –5.15 mA	1.25		
		O_{64}, O_{74}, B_{64} outputs		I_{OH} = = –4 mA	1.53		
		O_{24}, B_{34} outputs	V_{CC} = 2.5 V,	I_{OH} = = –6.2 mA	1.7		
		B_{38} outputs		I_{OH} = –12.4 mA	1.7		
		B_{38} outputs		I_{OH} = –10.57 mA	2.4		
		B_{38} outputs	V_{CC} = 3.3 V,	I_{OH} = –10.57 mA	1.25		
		O_{24}, B_{34} outputs		I_{OH} = –-5.29 mA	2.4		
V_{OL}	Low-level output voltage	O_{64}, O_{74}, B_{64} outputs	V_{CC} = 1.8 V,	I_{OL} = 4 mA		0.19	V
		O_{14}, O_{24}, B_{14}, B_{34} outputs		I_{OL} = 2.89 mA		0.4	
		B_{18}, B_{38} outputs		I_{OL} = 5.72 mA		0.4	
		O_{58} outputs		I_{OL} = 5.78 mA		0.4	
		O_{24}, B_{34} outputs	V_{CC} = 2.5 V,	I_{OL} = 6.3 mA		0.7	
		B_{38} outputs		I_{OL} = 12.7 mA		0.7	
		O_{24}, B_{34} outputs	V_{CC} = 3.3 V,	I_{OL} = 9.38 mA		0.4	
		B_{38} outputs		I_{OL} = 18.68 mA		0.4	

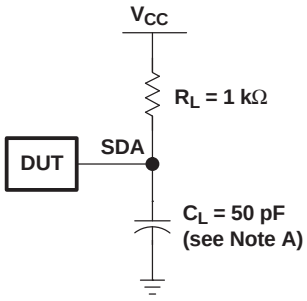
Interface Timing Requirements

This section defines the timing requirements for the external interfaces for the DLPC300 Controller.

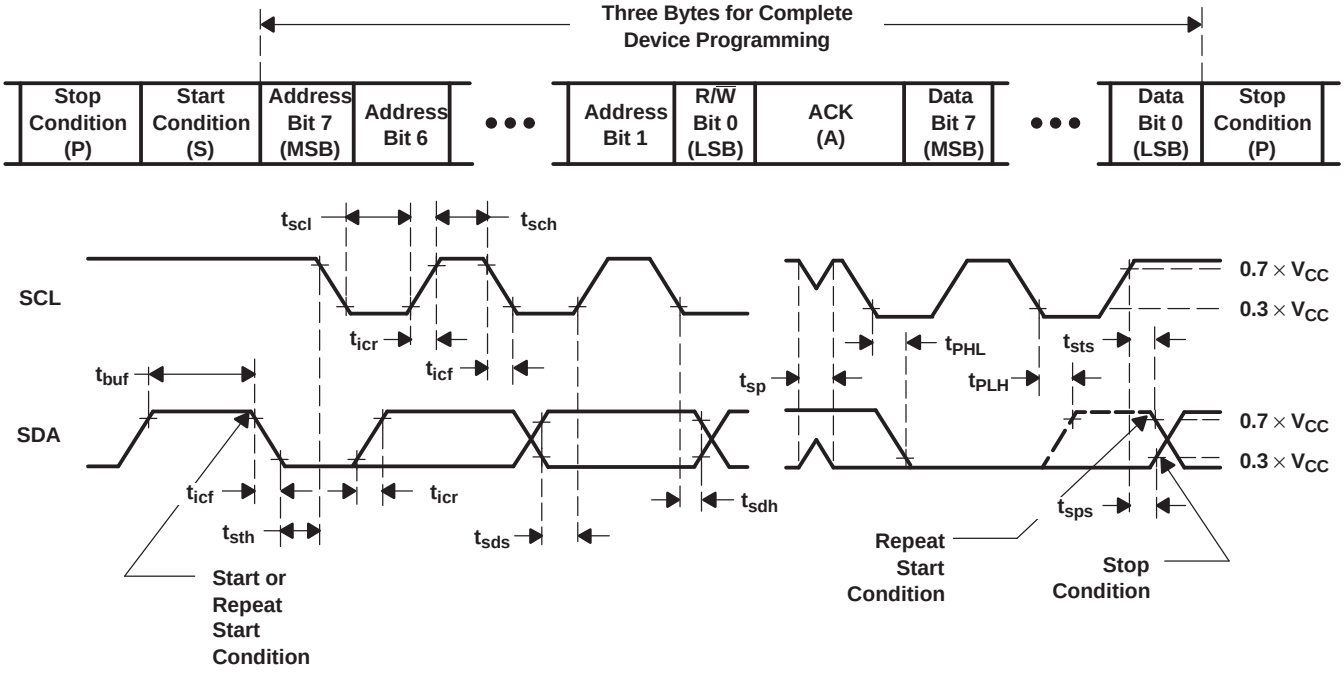
I²C Electrical Data/Timing

Table 7. I²C INTERFACE TIMING REQUIREMENTS

PARAMETER			MIN	MAX	UNIT
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		1		ms
t_{scl}	I²C clock low time		1		ms
t_{sp}	I²C spike time			20	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		100		ns
t_{icr}	I²C input rise time		100		ns
t_{ocf}	I²C output fall time	50 pF	30	200	ns
t_{buf}	I²C bus free time between stop and start conditions		1.3		ms
t_{sts}	I²C start or repeat start condition setup		1		ms
t_{sth}	I²C start or repeat start condition hold		1		ms
t_{sph}	I²C stop condition setup		1		ms
t_{vd}	Valid-data time	SCL low to SDA output valid		1	ms
	Valid-data time of ACK condition	ACK signal from SCL low to SDA (out) low		1	ms
t_{sch}	I²C bus capacitive load		0	100	pF



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

A. C_L includes probe and jig capacitance.

Figure 10. I^2C Interface Load Circuit and Voltage Waveforms

Parallel Bus Interface

Parallel bus interface supports six data transfer formats:

- 16-bit RGB565
- 18-bit RGB666
- 18-bit 4:4:4 YCrCb666
- 24-bit RGB888
- 24-bit 4:4:4 YCrCb888

- 16-bit 4:2:2 YCrCb (standard sampling assumed to be Y0Cb0, Y1Cr0, Y2Cb2, Y3Cr2, Y4Cb4, Y5Cr4, …)

The required PDATA(23:0) bus mapping for these 6 data transfer formats are as shown in Figure 11 .

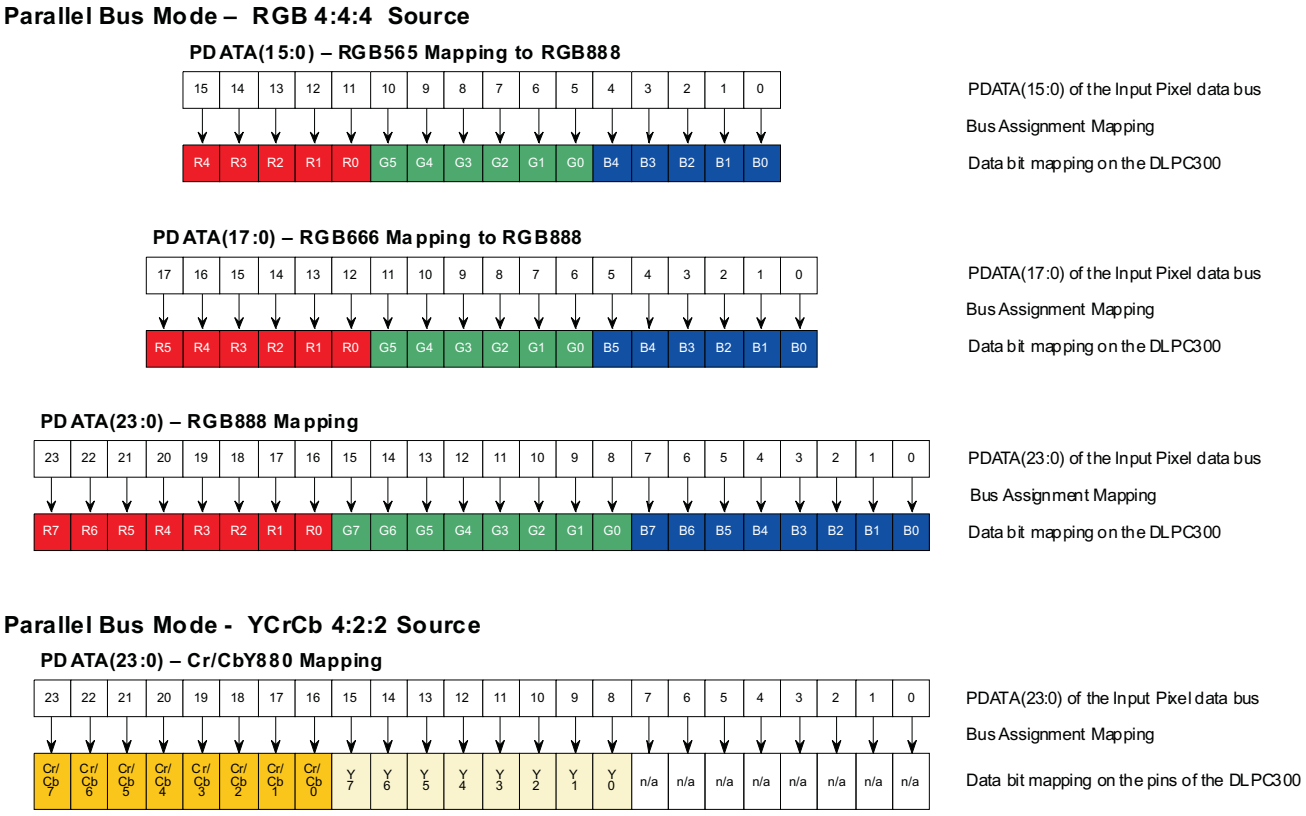


Figure 11. PDATA Bus – Parallel I/F Mode Bit Mapping

The parallel bus interface complies with the standard graphics interface protocol, which includes a vertical sync signal (VSYNC), horizontal sync signal (HSYNC), optional data-valid signal (DATAEN), a 24-bit data bus (PDATA), and a pixel clock (PCLK). The polarities of both syncs are programmable, as is the active edge of the clock. The relationship of these signals is shown in Figure 12. The data-valid signal (DATAEN) is optional, in that the DLPC300 provides auto-framing parameters that can be programmed to define the data-valid window, based on pixel and line counting relative to the horizontal and vertical syncs.

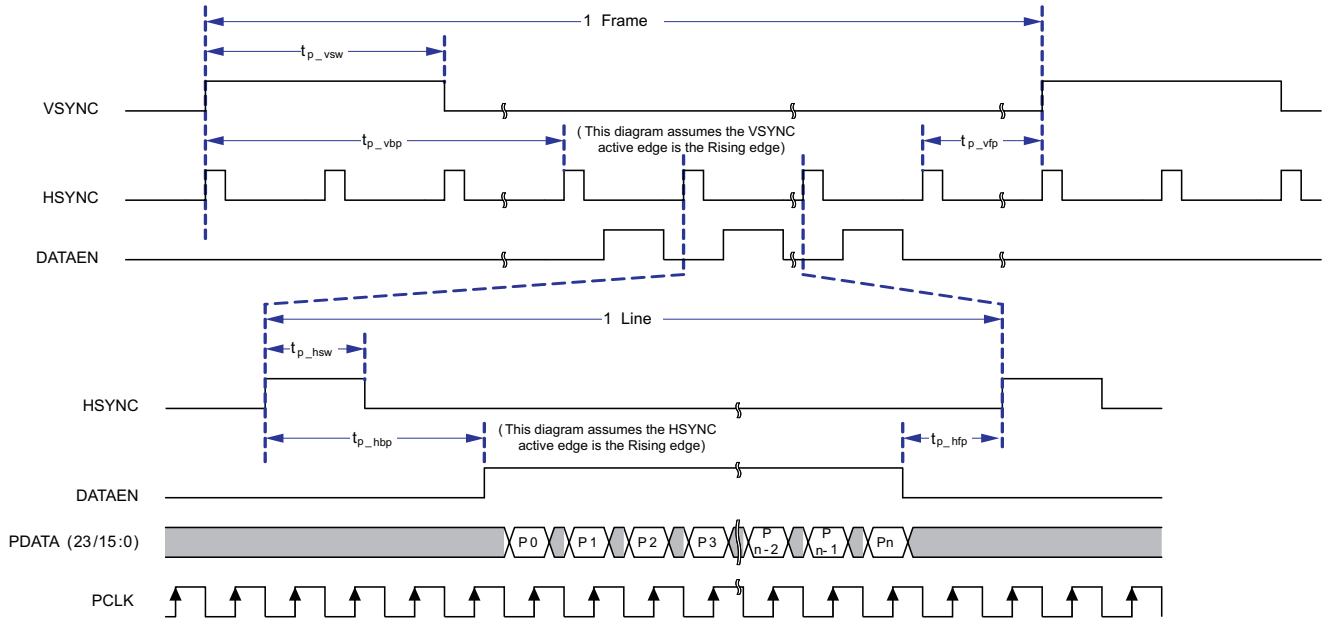


Figure 12. Parallel I/F Frame Timing

Table 8. Parallel Interface Frame Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{p_vsw}	Pulse duration – VSYNC high	50% reference points	1		lines
t_{p_vbp}	Vertical back porch – time from the leading edge of VSYNC to the leading edge HSYNC for the first active line(1)	50% reference points	2		lines
t_{p_vfp}	Vertical front porch – time from the leading edge of the HSYNC following the last active line in a frame to the leading edge of VSYNC(1)	50% reference points	1		lines
t_{p_tvb}	Total vertical blanking – time from the leading edge of HSYNC following the last active line of one frame to the leading edge of HSYNC for the first active line in the next frame. [This is equal to the sum of vertical back porch (t_{p_vbp}) + vertical front porch (t_{p_vfp})]	50% reference points	12		lines
t_{p_hsw}	Pulse duration – HSYNC high	50% reference points	4	128	PCLKs
t_{p_hbp}	Horizontal back porch – time from rising edge of HSYNC to rising edge of DATAEN	50% reference points	4		PCLKs
t_{p_hfp}	Horizontal front porch – time from falling edge of DATAEN to rising edge of HSYNC	50% reference points	8		PCLKs
t_{p_thh}	Total horizontal blanking – sum of horizontal front and back porches(2)	50% reference points			PCLKs

(1) The programmable parameter *Vertical Sync Line Delay* (I^2C: 0x23) must be set such that: 6 – *Vertical Front Porch* (t_{p_vfp}) (min 0) ≤ *Vertical Sync Line Delay* ≤ *Vertical Back Porch* (t_{p_vbp}) -2 (max 15). The default value for *Vertical Sync Line Delay* is set to 5; thus, only a *Vertical Back Porch* less than 7 requires potential action.

(2) Total horizontal blanking is driven by the maximum line rate for a given source, which is a function of resolution and orientation. See Table 10 for the maximum line rate for each source/display combination. t_{p_thb} = Roundup[(1000 × f_{clock})/LR] – APPL where f_{clock} = pixel clock rate in MHz, LR = line rate in kHz and APPL is the number of active pixels per (horizontal) line. If t_{p_thb} is calculated to be less than t_{p_hbp} + t_{p_hfp}, then the pixel clock rate is too low or the line rate is too high and one or both must be adjusted.

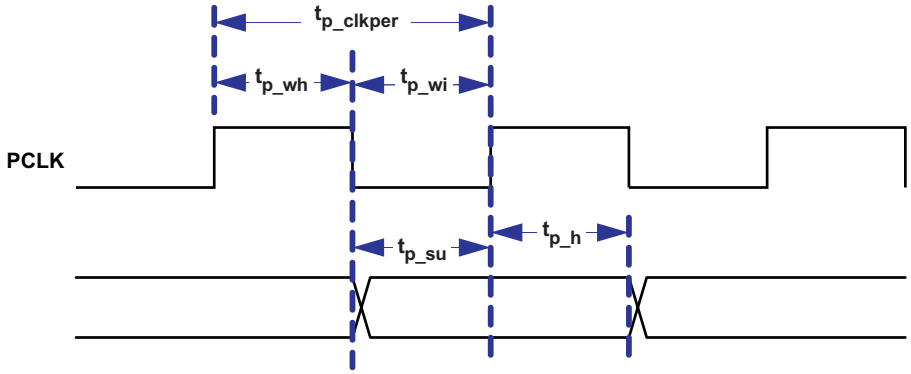


Figure 13. Parallel and BT.656 I/F General Timing

Table 9. Parallel Interface General Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		1	33.5	MHz
t_{p_clkper}	Clock period, PCLK	50% reference points	29.85	1,000	ns
t_{p_clkjit}	Clock jitter, PCLK (1)	Maximum f_{clock}			
t_{p_wh}	Pulse duration low, PCLK	50% reference points	10		ns
t_{p_wl}	Pulse duration high, PCLK	50% reference points	10		ns
t_{p_su}	Setup time – HSYNC, DATEN, PDATA(23:0) valid before the active edge of PCLK (2) (3)	50% reference points	3		ns
t_{p_h}	Hold time – HSYNC, DATEN, PDATA(23:0) valid after the active edge of PCLK (2) (3)	50% reference points	3		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	4	ns

(1) Clock jitter (in ns) should be calculated using this formula: Jitter = [1/ f_{clock} – 28.35 ns]. Setup and hold times must be met during clock jitter.
(2) The active (capture) edge of PCLK for HSYNC, DATEN and PDATA(23:0) is SW programmable but defaults to the rising edge.
(3) See Figure 13.

Table 10. Parallel I/F Maximum Supported Horizontal Line Rate

DMD	PARALLEL BUS SOURCE RESOLUTION	LANDSCAPE FORMAT (1)		PORTRAIT FORMAT (1)	
		RESOLUTION (H×V)	MAX LINE RATE (kHz)	RESOLUTION (H×V)	MAX LINE RATE (kHz)
0.3 WVGA diamond	NSTC (2)	720 × 240	17	Not supported	N/A
	PAL (2)	720 × 288	20	Not supported	N/A
	QVGA	320 × 240	17	240 × 320	22
	QWVGA	427 × 240	17	240 × 427 (2)	27
	3:2 VGA	640 × 430	30	430 × 640	45
	4:3 VGA	640 × 480	34	480 × 640	45
	WVGA-720	720 × 480	34	480 × 720	51
	WVGA-752	752 × 480	34	480 × 752	53
	WVGA-800	800 × 480	34	480 × 800	56
	WVGA-852	852 × 480	34	480 × 852	56
	WVGA-853	853 × 480	34	480 × 853	56
	WVGA-854	854 × 480	34	480 × 854	56
	WVGA-864	864 × 480	34	480 × 864	56
	Optical test	608 × 684	48	Not supported	N/A

(1) See the *DLPC300 Software Programmers Guide* (TI literature number DLPU004) to invoke the appropriate input and output resolutions.
(2) NTSC and PAL are assumed to be interlaced sources.

BT.656 Interface

The DLPC300 controller input interface supports the industry standard BT.656 parallel video interface. See the appropriate ITU-R BT.656 specification for detailed interface timing requirements.

Table 11. BT.565 I/F General Timing Requirements(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		1	33.5	MHz
t_{p_clkper}	Clock period, PCLK	50% reference points	29.85	1,000	ns
t_{p_clkjit}	Clock jitter, PCLK(2)	Maximum f_{clock}			
t_{p_wh}	Pulse duration low, PCLK	50% reference points	10		ns
t_{p_wl}	Pulse duration high, PCLK	50% reference points	10		ns
t_{p_su}	Setup time – HSYNC, DATEN, PDATA(23:0) valid before the active edge of PCLK	50% reference points	3		ns
t_{p_h}	Hold time – HSYNC, DATEN, PDATA(23:0) valid after the active edge of PCLK	50% reference points	3		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	4	ns

(1) The BT.656 I/F accepts 8-bit per color, 4:2:2 YCb/Cr data encoded per the industry standard via PDATA(7:0) on the active edge of PCLK (i.e., programmable) as shown in Figure 13.
(2) Clock jitter (in ns) should be calculated using this formula: Jitter = [1/ f_{clock} – 28.35 ns]. Setup and hold times must be met during clock jitter.

BT.656 data bits should be mapped to the DLPC300 PDATA bus as shown in Figure 14.

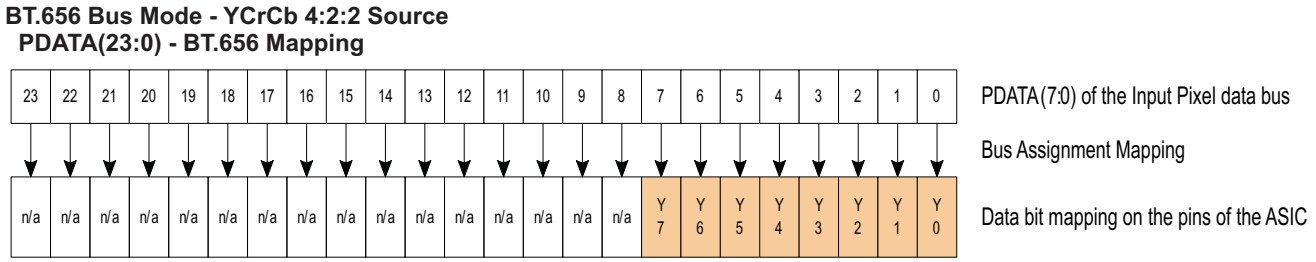


Figure 14. PDATA Bus – BT.656 I/F Mode Bit Mapping

Flash Memory Interface

DLPC300 uses an external 16-Mbit SPI serial flash slave memory device for configuration support. The contents of this flash memory can be downloaded from the DLPC300 product folder. The DLPC300 uses a single SPI interface, employing SPI mode 0 protocol, operating at a nominal frequency of 33.3 MHz.

When $\overline{\text{RESET}}$ is released, the DLPC300 reads the contents of the serial flash memory and executes an auto-initialization routine. During this time, GPIO4_INTF is set high to indicate auto-initialization is busy. Upon completion of the auto-initialization routine, the DLPC300 sets GPIO4_INTF low to indicate that the auto-initialization routine sucessfully completed.

The DLPC300 should support any flash device that is compatible with standard SPI mode 0 protocol and meet the timing requirement shown in Table 14. However, the DLPC300 does not support the normal (slow) read opcode, and thus cannot automatically adapt protocol and clock rate based on the electronic signature ID of the flash. The flash instead uses a fixed SPI clock and assumes certain attributes of the flash have been ensured by PCB design. The DLPC300 also assumes the flash supports address auto-incrementing for all read operations. The specific Instruction opcode and timing compatibility requirements for a DLPC300-compatible flash are listed in Table 12.

Table 12. SPI Flash Instruction OpCode and Timing Compatibility Requirements

SPI FLASH COMMAND	OPCODE (hex)	ADDRESS BYTES	DUMMY BYTES	CLOCK RATE
Fast READ (single output)	0x0B	3	1	33.3 MHz
All others	Can vary	Can vary	Can vary	33.3 MHz

The DLPC300 does not have any specific page, block or sector size requirements except that programming via the I^2C interface requires the use of page-mode programming. If, however, the user would like to dedicate a portion of the serial flash for storing external data (such as calibration data) and access it through the DLPC300's I^2C interface, then the minimum sector size must be considered, as it drives minimum erase size. Note that use of serial flash for storing external data may impact the number of features that can be supported in Table 13.

Note that the DLPC300 does not drive the $\overline{\text{HOLD}}$ (active-low hold) or $\overline{\text{WP}}$ (active-low write protect) pins on the flash device, and thus these pins should be tied to a logic high on the PCB via an external pullup.

The DLPC300 supports 1.8-, 2.5- or 3.3-V serial flash devices. To do so, VCC_FLSH must be supplied with the corresponding voltage. Table 13 contains a list of 1.8-, 2.5- and 3.3-V compatible SPI serial flash devices supported by DLPC300.

Table 13. Compatible SPI Flash Device Options(1)

DENSITY	VENDOR	PART NUMBER(2)	SUPPLY VOLTAGE SUPPORTED(3)	MIN CHIP SELECT HIGH TIME (t_{CSH})	MAX FAST READ FREQ(4)	TABLE 21 OPCODE AND TIMING COMPATIBLE
4 Mbit	Macronix	MX25U4035	1.65 V–2 V	30 ns	40 MHz	Yes
8 Mbit	Macronix	MX25U8035	1.65 V–2 V	30 ns	40 MHz	Yes
16 Mbit	Winbond	W25Q16BLxxxx	2.3 V–3.6 V	100 ns	50 MHz	Yes
8 Mbit	Macronix	MX25L8005ZUx-xxG	2.7 V–3.6 V	100 ns	66 MHz	Yes

(1) All the SPI devices listed have been verified to be compatible with DLPC300.
(2) Lower case *x* is used as a wild-card place holder and indicates an option that is selectable by the user. Note that the use of an upper case *X* is part of the actual part number.
(3) The flash supply voltage must match VCC_FLSH on the DLPC300. 1.8-V and 2.5-V SPI device options are limited. Special attention must be paid when ordering devices to be sure the desired supply voltage is attained, as multiple voltage options are often available under the same base part number.
(4) Maximum supported fast read frequency at the minimum supported supply voltage

Table 14. Flash Interface Timing Requirements(1)(2)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency, SPICLK(3)		33.3266	33.34	MHz
t_{p_clkper}	Clock period, SPICLK	50% reference points	29.994	30.006	ns
t_{p_wh}	Pulse duration low, SPICLK	50% reference points	10		ns
t_{p_wl}	Pulse duration high, SPICLK	50% reference points	10		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	4	ns
t_{p_su}	Setup time – SPIDIN valid before SPICLK falling edge	50% reference points	10		ns
t_{p_h}	Hold time – SPIDIN valid after SPICLK falling edge	50% reference points	0		ns
t_{p_clqv}	SPICLK clock low to output valid time – SPIDOUT and $\overline{\text{SPICS0}}$	50% reference points		1.0	ns
t_{p_clqx}	SPICLK clock low output hold time – SPI_DOUT and $\overline{\text{SPICS0}}$	50% reference points	–1		ns

(1) Standard SPI protocol is to transmit data on the falling edge of SPICLK and to capture data on the rising edge. The DLPC300 does transmit data on the falling edge, but it also captures data on the falling edge rather than the rising edge. This provides support for SPI devices with long clock-to-Q timing. DLPC300 hold capture timing has been set to facilitate reliable operation with standard external SPI protocol devices.
(2) With the above output timing, DLPC300 provides the external SPI device 14-ns input setup and 14-ns input hold relative to the rising edge of SPICLK.
(3) This range includes the 200 ppm of the external oscillator (but no jitter).

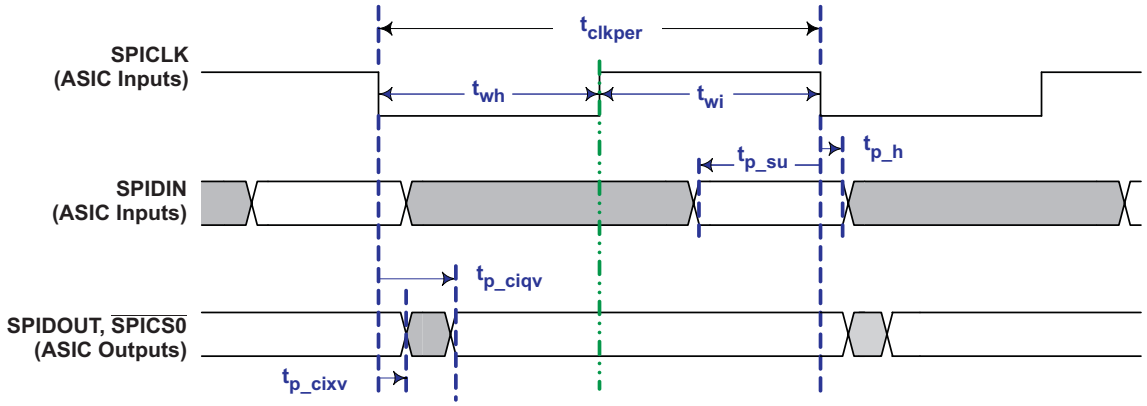


Figure 15. Flash Interface Timing

DMD Interface

The DLPC300 controller DMD interface consists of a 76.19-MHz (nominal) DDR output-only interface with LVCMOS signaling.

Table 15. DMD Interface Timing Requirements(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency, DMD_DCLK and DMD_SAC_CLK(2)		76.198	76.206	MHz
t_{p_clkper}	Clock period, DMD_DCLK and DMD_SAC_CLK	50% reference points	13.123	15	ns
t_{p_wh}	Pulse duration low, DMD_DCLK and DMD_SAC_CLK	50% reference points	6.2		ns
t_{p_wl}	Pulse duration high, DMD_DCLK and DMD_SAC_CLK	50% reference points	6.2		ns
t_t	Transition time – all signals	20% to 80% reference points	0.3	2	ns
t_{p_su}	Output setup time – DMD_D(14:0), DMD_SCTRL, DMD_LOADB and DMD_TRC relative to both rising and falling edges of DMD_DCLK(3)(4)	50% reference points		1.5	ns
t_{p_h}	Output hold time – DMD_D(14:0), DMD_SCTRL, DMD_LOADB and DMD_TRC signals relative to both rising and falling edges of DMD_DCLK(3)(4)	50% reference points		1.5	ns
$t_{p\_d1\_skew}$	DMD data skew – DMD_D(14:0), DMD_SCTRL, DMD_LOADB, and DMD_TRC signals relative to each other(5)	50% reference points		0.2	ns
$t_{p\_clk\_skew}$	Clock skew – DMD_DCLK and DMD_SAC_CLK relative to each other	50% reference points		0.2	ns
$t_{p\_d2\_skew}$	DAD/SAC data skew - DMD_SAC_BUS, DMD_DRC_OE, DMD_DRC_BUS, and DMD_DRC_STRB signals relative to DMD_SAC_CLK	50% reference points		0.2	ns

(1) Assumes a 30-Ω series termination for all DMD interface signals
(2) This range includes the 200 ppm of the external oscillator (but no jitter).
(3) Assumes minimum DMD setup time = 1 ns and minimum DMD hold time = 1 ns
(4) Output setup/hold numbers already account for controller clock jitter. Only routing skew and DMD setup/hold need be considered in system timing analysis.
(5) Assumes DMD data routing skew = 0.1 ns max

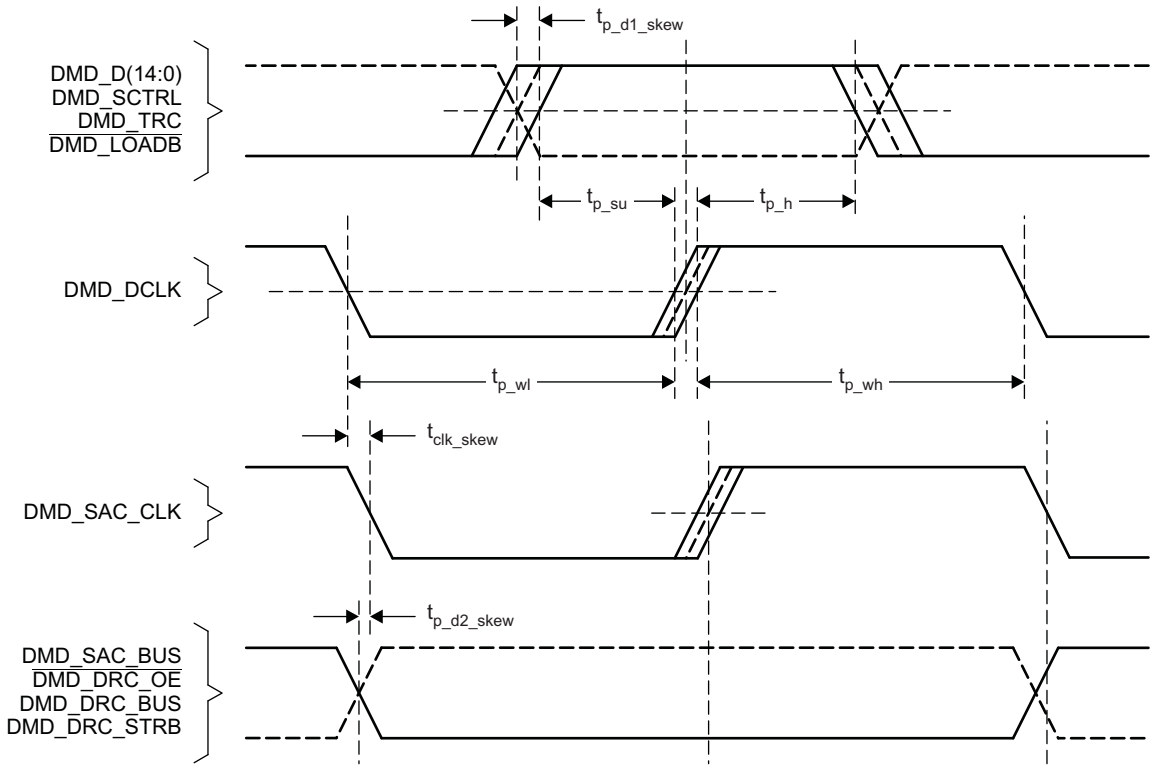


Figure 16. DMD Interface Timing

Mobile DDR Memory Interface

The DLPC300 stores bit plane data in external mobile dual data rate memory (mDDR). The mDDR compatibility requirements for the DLPC300 are:

- SDRAM memory type: Mobile-DDR
- Size: 128 Mbit minimum. DLPC300 can only address 128 Mb; use of larger memories requires bit A13 to be grounded.
- Organization: N × 16-bits wide with 4 equally sized banks
- Burst length: 4
- Refresh period: ≥ 64 ms
- Speed Grade t_{CK}: 6 ns max
- CAS latency (C_L), t_{RCD},t_{RP} parameters (clocks): 3, 3, 3

Table 16 shows the mobile-DDR DRAM devices recommended for use with the DLPC300.

Table 16. Compatible Mobile DDR DRAM Device Options(6)

VENDOR	PART NUMBER(7)	SIZE	ORGANIZATION	SPEED GRADE(8) (t_{CK})	CAS LATENCY (C_L) t_{RCD},t_{RP} PARAMETERS (CLOCKS)
Elpida	EDD25163HBH-6ELS-F	256 Mbit	16M × 16	6 ns	3, 3, 3
Samsung	K4X56163PN-FGC6	256 Mbit	16M × 16	6 ns	3, 3, 3
Micron	MT46H16M16LFBF-6IT:H	256 Mbit	16M × 16	6 ns	3, 3, 3
Hynix	H5MS2562JFR-J3M	256 Mbit	16M × 16	6 ns	3, 3, 3

The DLPC300 controller mobile DDR memory interface consists of a 16-bit wide, mobile DDR interface (i.e., LVCMOS signaling) operated at 133.33 MHz (nominal).

(6) All the SDRAM devices listed have been verified to be compatible with the DLPC300.
(7) These part numbers reflect a Pb-free package.
(8) A 6-ns speed grade corresponds to a 166-MHz mDDR device.

Table 17. Mobile DDR Memory Interface Timing Requirements(1)(2)(3)

PARAMETER		MIN	MAX	UNIT
t_{CYCLE}	Cycle-time reference	7500		ps
t_{CH}	CK high pulse duration(4)	2700		ps
t_{CL}	CK low pulse duration(4)	2700		ps
t_{DQSH}	DQS high pulse duration(4)	2700		ps
t_{DQSL}	DQS low pulse duration(4)	2700		ps
t_{WAC}	CK to address and control outputs active	–2870	2870	ps
t_{QAC}	CK to DQS output active		200	ps
t_{DAC}	DQS to DQ/DM output active	–1225	1225	ps
t_{DQSRS}	Input (read) DQS/ DQ skew(5)		1000	ps

(1) This includes the 200 ppm of the external oscillator (but no jitter).
(2) Output setup/hold numbers already account for controller clock jitter. Only routing skew and memory setup/hold must be considered in system timing analysis.
(3) Assumes a 30-Ω series termination on all signal lines
(4) CK and DQS pulse duration specs for the DLPC300 assume it is interfacing to a 166-MHz mDDR device. Even though these memories are only operated at 133.33 MHz, according to memory vendors, the rated t_{CK} spec (i.e., 6 ns) can be applied to determine minimum CK and DQS pulse duration requirements to the memory.
(5) Note that DQS must be within the t_{DQSRS} read data-skew window but need not be centered.

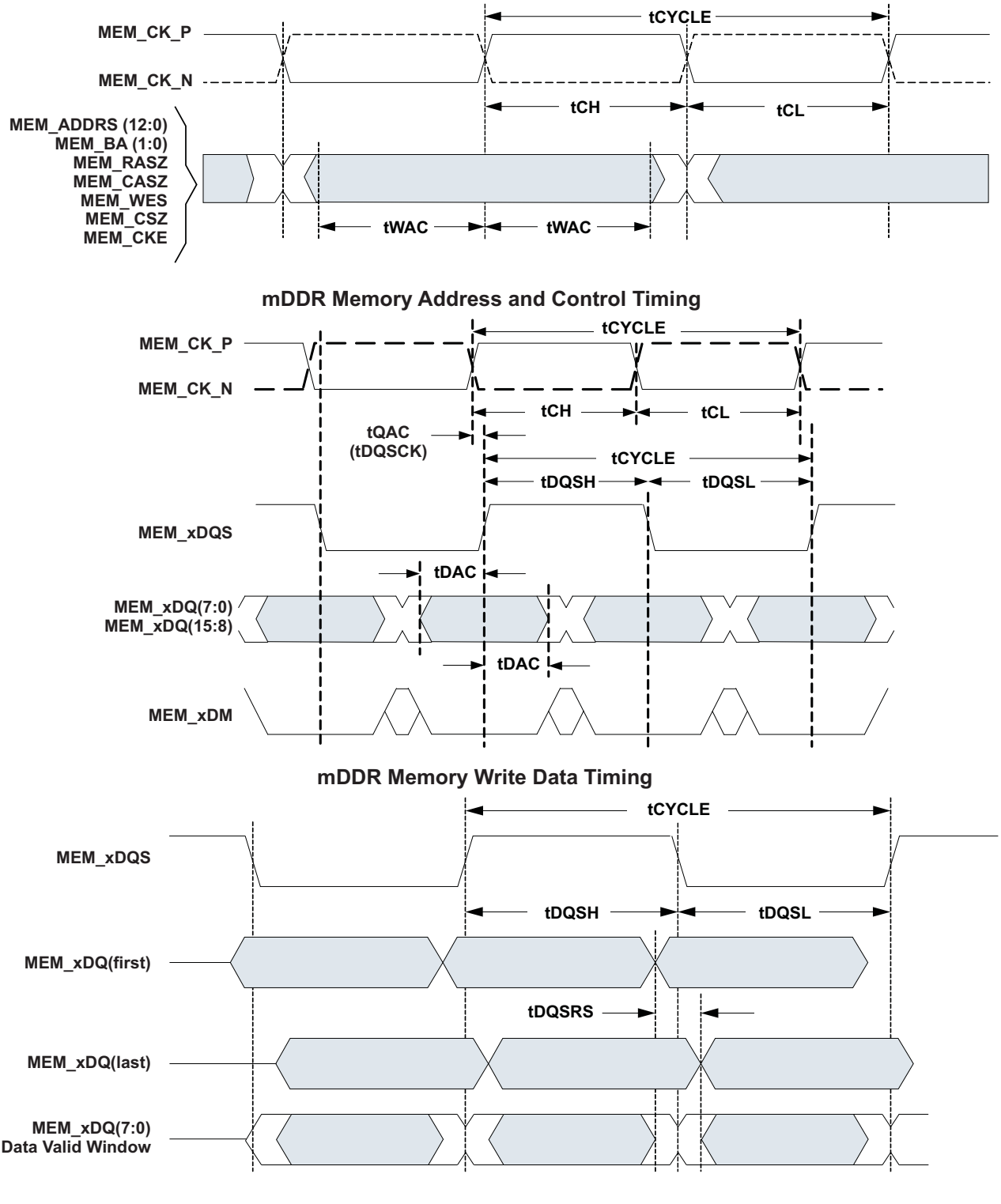


Figure 17. Mobile DDR Memory Interface Timing

Power-Up Initialization Sequence

It's assumed that an external power monitor holds the DLPC300 in system reset during power up. It must do this by driving RESET to a logic-low state. It should continue to assert system reset until all controller voltages have reached minimum specified voltage levels, PARK is asserted high, and input clocks are stable. During this time, most controller outputs are driven to an inactive state and all bidirectional signals are configured as inputs to avoid contention. Controller outputs that are not driven to an inactive state are in the high-impedance state. These include DMD_PWR_EN, LEDDVR_ON, LED_SEL_0, LED_SEL_1, SPICLK, SPIDOUT, and SPICS0. Once power is stable and the PLL_REFCLK clock input to the DLPC300 is stable, then RESET should be deactivated (set to a logic high). The DLPC300 then performs a power-up initialization routine that first locks its PLL followed by loading self-configuration data from the external flash. On release of RESET, all DLPC300 I/Os become active. Immediately following the release of RESET, the GPIO4_INTF signal is driven high to indicate that the auto initialization routine is in progress. On completion of the auto-initialization routine, the DLPC300 drives GPIO4_INTF low to signal INITIALIZATION DONE (also called INIT DONE).

Note that the host processor can start sending standard I^2C commands after GPIO4 (INIT_DONE) goes low, or a 100-ms timer expires in the host processor, whichever is earlier.

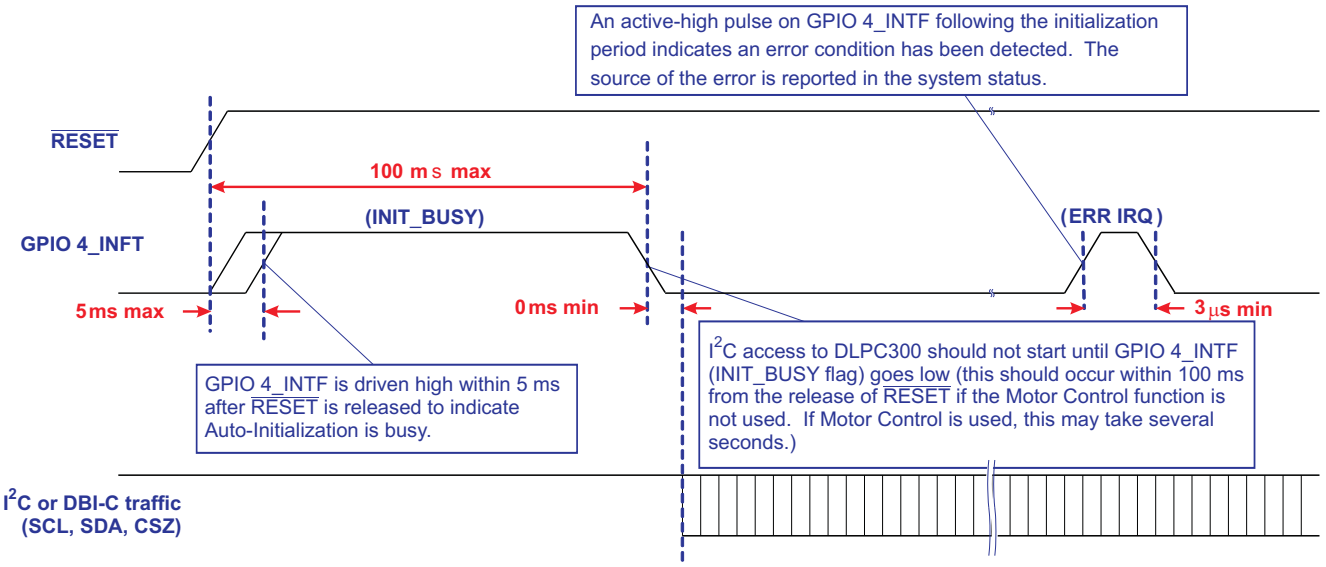


Figure 18. Initialization Timeline

System Power-Up/Down Sequence

Although the DLPC300 requires an array of power supply voltages, (e.g., VDD, VDD_PLL, VCC_18, VCC_FLSH, VCC_INTF), there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC300. This is true for both power-up and power-down scenarios. Similarly, there is no minimum time between powering up or powering down the different supplies feeding the DLPC300. Note, however, that it is not uncommon for there to be power-sequencing requirements for the devices that share the supplies with the DLPC300.

Although there is no risk of damaging the DLPC300 as a result of a given power sequence, from a functional standpoint there is one specific power-sequencing recommendation to ensure proper operation. In particular, all controller power should be applied and allowed to reach minimum specified voltage levels before RESET is de-asserted to ensure proper power-up initialization is performed. All I/O power should remain applied as long as 1-V core power is applied and RESET is de-asserted.

Note that when VDD10 core power is applied but I/O power is not applied, additional leakage current may be drawn.

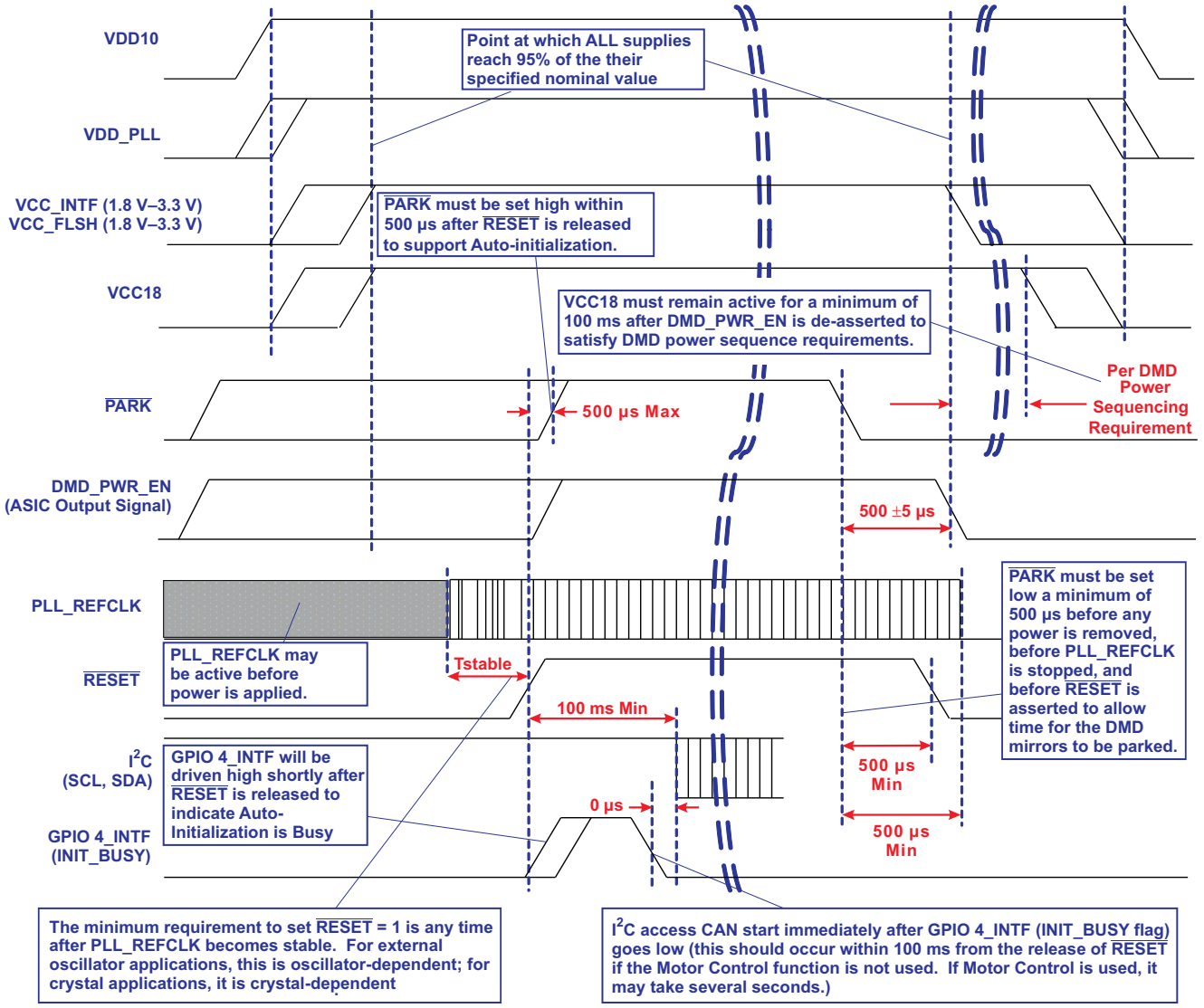


Figure 19. Power-Up/Down Timing

System Power I/O State Considerations

Note that:

- If VCC18 I/O power is applied when VDD10 core power is not applied, then all mDDR (non fail-safe) and non-mDDR (fail-safe) output signals associated with the VCC18 supply are in a high-impedance state.
- If VCC_INTF or VCC_FLSH I/O power is applied when VDD10 core power is not applied, then all output signals associated with these inactive I/O supplies are in a high-impedance state.
- If VDD10 core power is applied but VCC_INTF or VCC_FLSH I/O power is not applied, then all output signals associated with these inactive I/O supplies are in a high-impedance state.
- If VDD10 Core power is applied but VCC18 I/O power is not applied,, then all mDDR (non fail-safe) and non-mDDR (fail-safe) output signals associated with the VCC18 I/O supply are in a high-impedance state; however, if driven high externally, only the non-mDDR (fail-safe) output signals remain in a high-impedance state, and the mDDR (non fail-safe) signals are shorted to ground through clamping diodes.

Power-Good ($\overline{\text{PARK}}$) Support

The $\overline{\text{PARK}}$ signal is defined to be an early warning signal that should alert the controller 500 µs before dc supply voltages have dropped below specifications. This allows the controller time to park the DMD, ensuring the integrity of future operation. Note that the reference clock should continue to run and $\overline{\text{RESET}}$ should remain de-activated for at least 500 µs after $\overline{\text{PARK}}$ has been deactivated (set to a logic low) to allow the park operation to complete.

Hot-Plug Usage

Note that the DLPC300 provides fail-safe I/O on all host-interface signal (signals powered by VCC_INTF). This allows these inputs to be driven high even when no I/O power is applied. Under this condition, the DLPC300 does not load the input signal nor draw excessive current that could degrade controller reliability. Thus for example, the I^2C bus from the host to other components would not be affected by powering off VCC_INTF to the DLPC300. Note that weak pullups or pulldowns are recommended on signals feeding back to the host to avoid floating inputs.

Maximum Signal Transition Time

Unless otherwise noted, the maximum recommended 20%–80% rise/fall time to avoid input buffer oscillation is 10 ns. This applies to all DLPC300 input signals. Note, however, that the $\overline{\text{PARK}}$ input signal includes an additional small digital filter that ignores any input-buffer transitions caused by a slower rise/ fall time for up to 150 ns.

Configuration Control

The primary configuration control mechanism for the DLPC300 is the I^2C interface. See the *DLPC300 Software Programmer's Guide*, TI Literature Number DLPU004, for details on how to configure and control the DLPC300.

Thermal Considerations

The underlying thermal limitation for the DLPC300 is that the maximum operating junction temperature (T_J) not be exceeded (see Recommended Operating Conditions). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC300, and power dissipation of surrounding components. The DLPC300 package is designed primarily to extract heat through the power and ground planes of the PCB, thus copper content and airflow over the PCB are important factors.

Table 18. Package Thermal Resistance

PARAMETER		MIN	NOM	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case			19.52	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-air, with no forced airflow			64.96	°C/W

External Clock Input Crystal Oscillator

The DLPC300 requires an external reference clock to feed its internal PLL. This reference may be supplied via a crystal or oscillator. The DLPC300 accepts a reference clock of 16.667 MHz with a maximum frequency variation of 200 ppm (including aging, temperature and trim component variation). When a crystal is used, several discrete components are also required as shown in Figure 20.

CL = Crystal load capacitance (Farads)
CL1 = 2 * (CL – Cstray_pll_refclk_i)
CL2 = 2 * (CL – Cstray_pll_refclk_o)

Where:
Cstray_pll_refclk_i = Sum of package and PCB srtay capacitance at the crystal pin associated with the ASIC pin pll_refclk_i.
Cstray_pll_refclk_o = Sum of package and PCB srtay capacitance at the crystal pin associated with the ASIC pin pll_refclk_o.

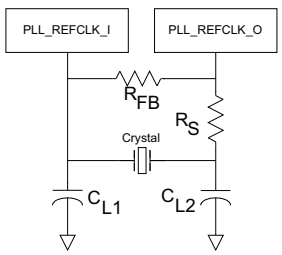


Figure 20. Recommended Crystal Oscillator Configuration

Table 19. Crystal Port Electrical Characteristics

PARAMETER	NOM	UNIT
PLL_REFCLK_I TO GND capacitance	4.5	pF
PLL_REFCLK_O TO GND capacitance	4.5	pF

Table 20. Recommended Crystal Configuration

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	16.667	MHz
Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity)	±200	PPM
Crystal drive level	100 max	uW
Crystal equivalent series resistance (ESR)	80 max	Ω
Crystal load	12	pF
R_S drive resistor (nominal)	100	Ω
R_{FB} feedback resistor (nominal)	1	MΩ
C_{L1} external crystal load capacitor	See Figure 20	pF
C_{L2} external crystal load capacitor	See Figure 20	pF
PCB layout	A ground isolation ring around the crystal is recommended	

If an external oscillator is used, then the oscillator output must drive the PLL_REFCLK_I pin on the DLPC300 controller, and the PLL_REFCLK_O pins should be left unconnected. The benefit of an oscillator is that it can be made to provide a spread-spectrum clock that reduces EMI. Note, however, that the DLPC300 can only accept between 0% to –2% spreading (i.e., down spreading only) with a modulation frequency between 20kHz and 65 KHz and a triangular waveform.

Similar to the crystal option, the oscillator input frequency is limited to the 16.667 MHz.

It iss assumed that the external crystal or oscillator stabilizes within 50 ms after stable power is applied.

PLL

The DLPC300 contains one internal PLL that has a dedicated analog supply (VDD_PLL , VSS_PLL). As a minimum, the VDD_PLL power and VSS_PLL ground pins should be isolated using an RC-filter consisting of two 50-Ω series ferrites and two shunt capacitors (to widen the spectrum of noise absorption). It is recommended that one capacitor be a 0.1-µf capacitor and the other be a 0.01-µf capacitor. All four components should be placed as close to the controller as possible, but it is especially important to keep the leads of the high-frequency capacitors as short as possible. Note that both capacitors should be connected across VDD_PLL and VSS_PLL on the controller side of the ferrites.

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, VDD_PLL must be a single trace from the DLPC300 to both capacitors and then through the series ferrites to the power source. The power and ground traces should be as short as possible, parallel to each other and as close as possible to each other.

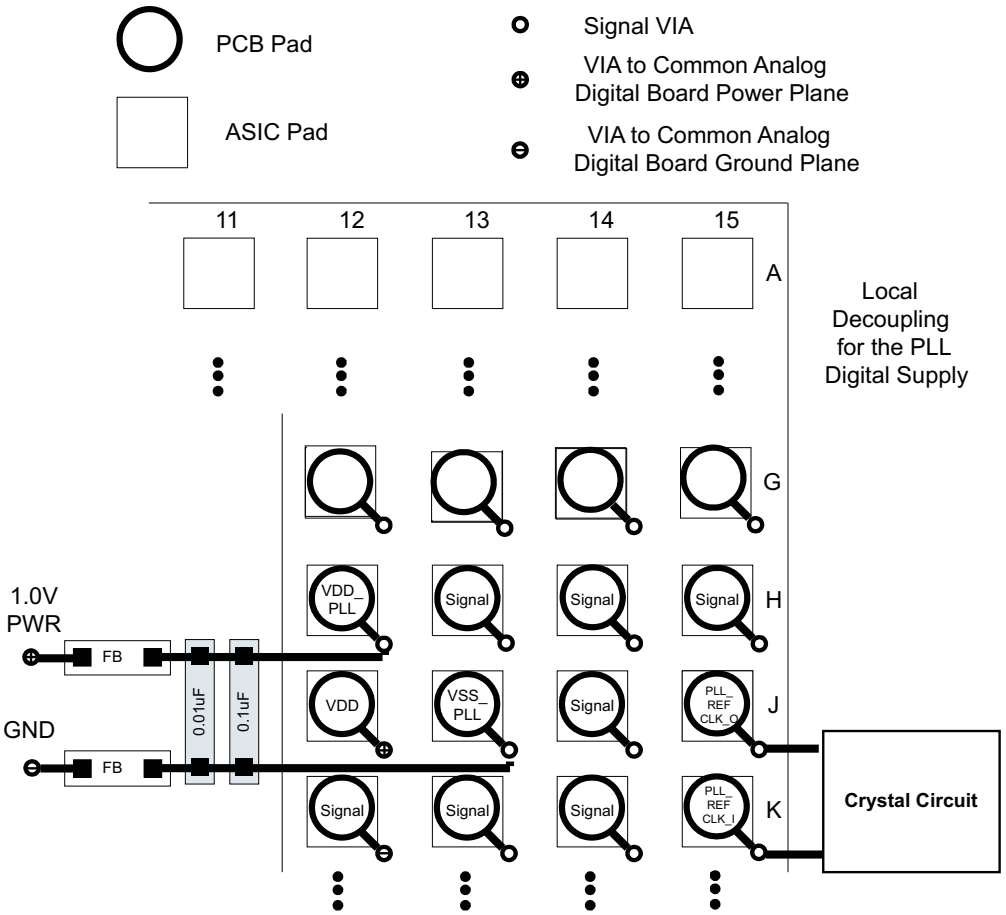


Figure 21. PLL Filter Layout

General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, it is recommended that unused controller input pins be tied through a pullup resistor to its associated power supply or through a pulldown to ground. For controller inputs with internal pullup or pulldown resistors, it is unnecessary to add an external pullup/pulldown unless specifically recommended. Note that internal pullup and pulldown resistors are weak and should not be expected to drive the external line. The DLPC300 implements very few internal resistors and these are noted in the pin list.

Unused output-only pins can be left open.

When possible, it is recommended that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they should be pulled up (or down) using an appropriate resistor.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DLPC300ZVB	ACTIVE	NFBGA	ZVB	176	10	Pb-Free (RoHS)	Call TI	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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